



2.2 Catering to Student Diversity

2.2.1 The institution assesses the learning levels of the students and organizes special programmes for advanced learners and slow learners

Table of Contents

Sl.No.	Contents	Page No.
1	Orientation Program	2
2	Bright/Weak student list	9
3	Participation certificates of students in various events- Tech Fest, Hackathon, Webinars, Workshops, Conferences and Online courses	11
4	Student membership in professional Body	<u>26</u>
5	Gate Coaching	<u>34</u>
6	Funded projects	38
7	Appreciation to Best outgoing student and university rank holders	40
8	Remedial Class	46
9	University Question paper and Answer Key	51
10	Handout Copy	55
11	Workshops, Talks conducted in VJCET	57
12	Placement Activities	66
13	Club Activities	70
14	Lab manual copy	75
15	Activities in FAB Lab	<u>85</u>

Established in 2001 Managed by Catholic Diocese Kothamangalam



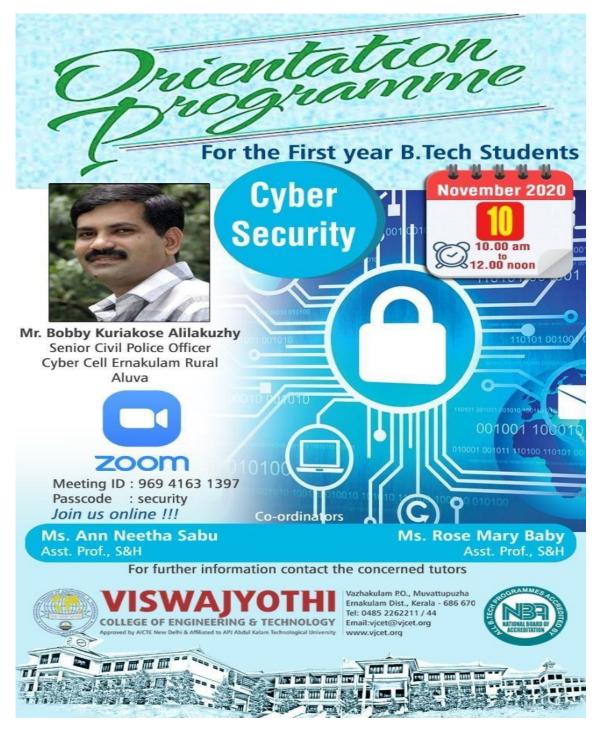
1. Orientation program

The college organizes an orientation program for students at the commencement of new batch every year. It helps students to get familiarized with the institution, curricular and cocurricular activities, facilities, rules and regulations.



Established in 2001 Managed by Catholic Diocese Kothamangalam

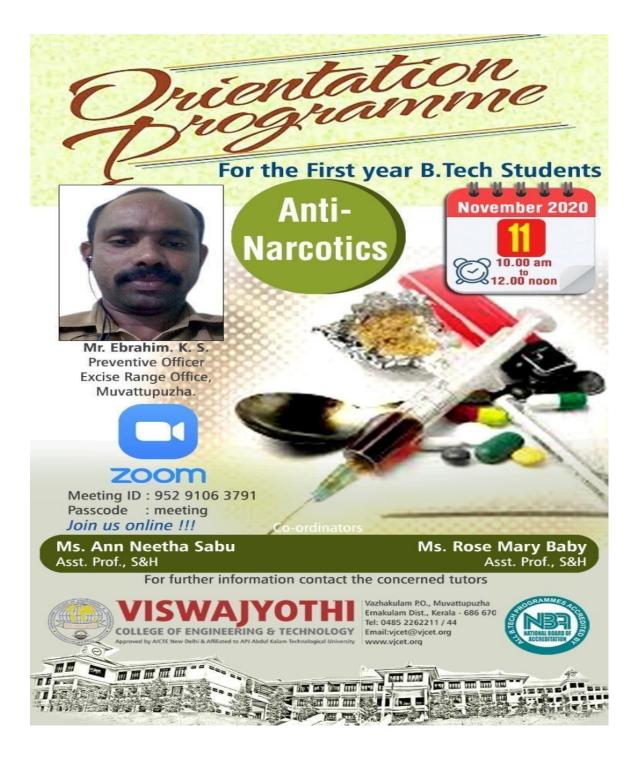






Established in 2001





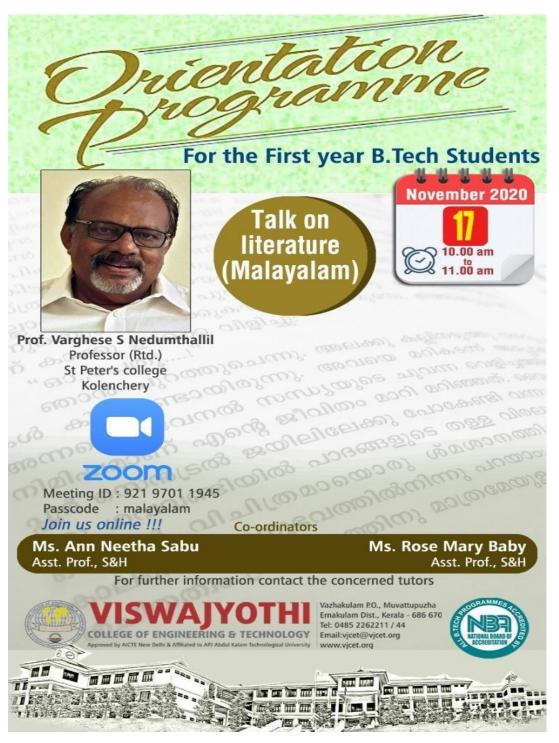
Established in 2001 Managed by Catholic Diocese Kothamangalam





Established in 2001 Managed by Catholic Diocese Kothamangalam





Established in 2001



DATE &			101	FIRST YEAR	STUDENT IND	UCTION PROG	RAM -2019-20 O	GY, VAZHAKUL DDD SEMESTER			
DAY	1	S1 CE A	S1 CE B	S1 CS A	S1 CS B	S1 EEE	S1 EC A	S1 EC B	S1 IT	S1 ME A	S1 ME B
7/2619 NDAT	3	GENERAL MEETING	GENERAL MEETING	GENERAL MEETING	GENERAL MEETING	GENERAL MEETING	GENERAL MEETING	GENERAL MEETING	GENERAL MEETING	GENERAL MEETING	GENERAL MEETING
TO/22 MOM	6 7	ноо/титоя	ноо/титоя	нор/титоя	HOD/TUTOR	нор/гитоя	HOD/TUTOR	нор/титоя	HOD/TUTOR	ноо/титоя	нор/титоя
	1 2			GOAL SETTING (GEO BABY)	GOAL SETTING (GEO BABY)				46,410		
23/67/2019 TUESDAY	3	PLACEMENT TRAINING	PLACEMENT TRAINING	FOREIGN LANGUAGE	FOREIGN LANGUAGE	TECHNICAL SKILL DEVELOPMENT (RABBITSQUARE)	PLACEMENT TRAINING	PLACEMENT TRAINING	PLACEMENT TRAINING	TECHNICAL SKILL DEVELOPMENT (RABBITSQUARE)	TECHNICAL SKILL DEVELOPMENT (RABBITSQUARE)
	6			FAB LAB	LIBRARY						
	7	ARTS & SPORTS	ARTS & SPORTS	ARTS & SPORTS	ARTS & SPORTS	ARTS & SPORTS	ARTS & SPORTS	ARTS & SPORTS	ARTS & SPORTS	ARTS & SPORTS	ARTS & SPORTS
24/07/2019 WEDNESDAY	1 2 3 4 5	PLACEMENT TRAINING	PLACEMENT TRAINING	TECHNICAL SKILL DEVELOPMENT (RABBITSQUARE)	TECHNICAL SKILL DEVELOPMENT (RABBITSQUARE)	FAB LAB INTRO TO SCIENTIFIC CALCULATOR (AJ) INTRO TO KTU (ANR)	PLACEMENT TRAINING	PLACEMENT TRAINING	PLACEMENT TRAINING	HOD/TUTOR INTRO TO SCIENTIFIC CALCULATOR (ANS) LIBRARY FABILAB	HOD/TUTOR INTRO TO SCIENTIFIC CALCULATOR (INT) INTRO TO ELEMENTARY MATHEMATICS (INT) ENERGY MANAGEMENT(AK) LIBRARY
	6		F100 100 100 100 100 100 100 100 100 100	100 C	20 10 10 10 10 10 10 10 10 10 10 10 10 10			700000000000000000000000000000000000000			
	1	GOAL SETTING (GEO BABY)	GOAL SETTING (GEO BABY)	ARTS & SPORTS	ARTS & SPORTS	ARTS & SPORTS	ARTS & SPORTS	ARTS & SPORTS	ARTS & SPORTS INTRO TO KTU (ANR)	ARTS & SPORTS	ARTS & SPORTS
25/07/2019 THURSDAY	3	INTRO TO KTU (ANR) HOD/TUTOR	LIBRARY	PLACEMENT TRAINING	PLACEMENT TRAINING	PLACEMENT TRAINING	TECHNICAL SKILL DEVELOPMENT (RABBITSQUARE)	TECHNICAL SKILL DEVELOPMENT (RABBITSQUARE)	ENERGY MANAGEMENT(AK) INTRO TO ELEMENTARY MATHEMATICS (DS)	PLACEMENT TRAINING	PLACEMENT TRAINING
THUM	5	FOREIGN LANGUAGE	FOREIGN LANGUAGE				(multi-scorne)	(Manual Scotte)	FAII LAII		
26/07/2019 FRIDAY	7	ARTS & SPORTS	ARTS & SPORTS	ARTS & SPORTS	ARTS & SPORTS	ARTS & SPORTS	ARTS & SPORTS	ARTS & SPORTS	ARTS & SPORTS	ARTS & SPORTS	ARTS & SPORTS
	2						FOREIGN LANGUAGE	FOREIGN LANGUAGE			
	4	TECHNICAL SKILL DEVELOPMENT (RABBITSQUARE)	TECHNICAL SKILL DEVELOPMENT (RABBITSQUARE)	PLACEMENT TRAINING	PLACEMENT TRAINING	PLACEMENT TRAINING	INTRO TO SCIENTIFIC CALCULATOR (JNT) ENERGY MANAGEMENT(AK)	LIBRARY	TECHNICAL SKILL DEVELOPMENT (RABBITSQUARE)	PLACEMENT TRAINING	PLACEMENT TRAINING
	6						LIBRARY	FAB LAB			
	7	ARTS & SPORTS	ARTS & SPORTS	ARTS & SPORTS	ARTS & SPORTS	ARTS & SPORTS	ARTS & SPORTS	ARTS & SPORTS	ARTS & SPORTS	ARTS & SPORTS	ARTS & SPORTS
	1	Talk on ANTI-NARCOTICS	Talk on ANTI-NARCOTICS	Talk on ANTI-NARCOTICS	Talk on ANTI-NARCOTICS	Talk on ANTI-NARCOTICS	Talk on ANTI-NARCOTICS	Talk on ANTI-NARCOTICS	Talk on ANTI-NARCOTICS	Talk on ANTI-NARCOTICS	Talk on ANTI-NARCOTIC
MONDAT	3 4	YOGA CLASS	YOGA CLASS	YOGA CLASS	YOGA CLASS	YOGA CLASS	YOGA CLASS	YOGA CLASS	YOGA CLASS	YOGA CLASS	YOGA CLASS
2	5	LIBRARY	INTRO TO KTU (ANR) SPOKEN TUTORIAL	KTU DATA ENTRY	SPOKEN TUTORIAL INTRO TO SCIENTIFIC	FOREIGN LANGUAGE	ETHICS & HUMAN VALUES	KTU DATA ENTRY	FOREIGN LANGUAGE	KTU DATA ENTRY	FAB LAS
	,	ARTS & SPORTS	ARTS & SPORTS	ARTS & SPORTS	ARTS & SPORTS	ARTS & SPORTS	ARTS & SPORTS	ARTS & SPORTS	ARTS & SPORTS	ARTS & SPORTS	ARTS & SPORTS
	2	KTU DATA ENTRY	ENERGY MANAGEMENT(AK) DEPARTMENT ACTIVITIES	INTRO TO SCIENTIFIC CALCULATOR (ANS) DEPARTMENT ACTIVITIES	INTRO TO ELEMENTARY MATHEMATICS (AJ)	KTU DATA ENTRY	FAB LAB	INTRO TO SCIENTIFIC CALCULATOR (DS) INTRO TO ELEMENTARY MATHEMATICS (DS)	ETHICS & HUMAN VALUES	INTRO TO KTU (ANR) SPOKEN TUTORIAL	KTU DATA ENTRY
TUESDAY	3	FAB LAB	KTU DATA ENTRY	INTRO TO ELEMENTARY MATHEMATICS (ANS) INTRO TO KTU	KTU DATA ENTRY	GOAL SETTING (GEO BABY)	KTU DATA ENTRY	ENERGY MANAGEMENT(AK) SPOKEN TUTORIAL	GOAL SETTING (GEO BABY)	FOREIGN LANGUAGE	FOREIGN LANGUAGE
2	5	DEPARTMENT ACTIVITIES	INTRO TO SCIENTIFIC CALCULATOR (AJ)	(ANR) ENERGY MANAGEMENT(AK)	TUTDR/HOD	DEPARTMENT ACTIVITIES	INTRO TO KTU (ANR)	TUTOR/HOD	INTRO TO SCIENTIFIC CALCULATOR (DS)	INTRO TO ELEMENTARY MATHEMATICS (ANS)	INTRO TO SCIENTIFIC CALCULATOR (INT)
	7	ROAD SAFTEY CLASS	ROAD SAFTEY CLASS	ROAD SAFTEY CLASS	ROAD SAFTEY CLASS	ROAD SAFTEY CLASS	ROAD SAFTEY CLASS	ROAD SAFTEY CLASS	ROAD SAFTEY CLASS	ROAD SAFTEY CLASS	ROAD SAFTEY CLASS
HI/O7/2019 WEDNESDAT						HOLIDAY (KAR	KIDAKAVAVU)				
3	1 2	DEPARTMENT ACTIVITIES INTRO TO SCIENTIFIC	INTRO TO ELEMENTARY MATHEMATICS (AJ)	TUTOR/HOD DEPARTMENT ACTIVITIES	FABLAB	TUTOR/HOD DEPARTMENT ACTIVITIES	INTRO TO ELEMENTARY MATHEMATICS (INT)	ETHICS & HUMAN VALUES	KTU DATA ENTRY	INTRO TO ELEMENTARY MATHEMATICS (ANS) ENERGY	SPOKEN TUTORIAL INTRO TO KTU
JOHA Y	,	TALK ON CYBER SECURITY		TALK ON CYBER SECURITY	TALK ON CYBER SECURITY	TALK ON CYBER SECURITY		TALK ON CYBER SECURITY	TALK ON CYBER SECURITY	MANAGEMENT(AK) TALK ON CYBER SECURITY	(ANR) TALK ON CYBER SECURITY
1/8/2018 THURSDAY	1	RESEARCH & DEVELOPMENT	RESEARCH & DEVELOPMENT	RESEARCH & DEVELOPMENT	RESEARCH & DEVELOPMENT	RESEARCH & DEVELOPMENT	RESEARCH & DEVELOPMENT	RESEARCH & DEVELOPMENT	RESEARCH & DEVELOPMENT	RESEARCH & DEVELOPMENT	RESEARCH & DEVELOPMENT
	9	START UP	START UP	START UP	START UP	START UP	START UP	START UP	START UP	START UP	START UP
	1 2	SPOKEN TUTORIAL ENERGY MANAGEMENTIAKI	HOD/TUTOR DEPARTMENT ACTIVITIES	KTU DATA ENTRY	DEPARTMENT ACTIVITIES	INTRO TO ELEMENTARY MATHEMATICS (AI)	KTU DATA ENTRY	INTRO TO KTU (ANR) INTRO TO ELEMENTARY	TUTOR/HOD SPOKEN TUTORIAL	ETHICS & HUMAN VALUES	KTU DATA ENTRY
2/N/Z01S FRIDAY	3	MANAGEMENT(AK) ETU DATA ENTRY	FABILAB	LIBRARY	INTRO TO ETU (ANR) ENERGY MANAGEMENT(AK)	KTU DATA ENTRY	TUTOR/HOD SPOKEN TUTORIAL	MATHEMATICS (DS) KTU DATA ENTRY	KTU DATA ENTRY	GOAL SETTING (GEO BABY)	GOAL SETTING (GEO BABY)
2=	3	INTRO TO ELEMENTARY MATHEMATICS (INT)	KTU DATA ENTRY	SPOKEN TUTORIAL INTRO TO ELEMENTARY MATHEMATICS (ANS)	KTU DATA ENTRY	SPOKEN TUTORIAL ENERGY MANAGEMENT(AK)	GOAL SETTING (GEO BABY)	GOAL SETTING (GEO BABY)	LIBRARY	KTU DATA ENTRY	ETHICS & HUMAN VALUES
		ARTS & SPORTS	ARTS & SPORTS	ARTS & SPORTS	ARTS & SPORTS	ARTS & SPORTS	ARTS & SPORTS	ARTS & SPORTS	ARTS & SPORTS	ARTS & SPORTS	ARTS & SPORTS

Established in 2001









Yoga class conducted on 29.07.2019

Established in 2001



2. Bright/Weak student list

•			VISWAJYOTHI COLL DEPARTMEN	T OF EL	ECTRIC	CAL AND	ELECTI	RONICS	OLOGY, ENGINEE	VAZI RING	IAKUL	AM		
		SERI	ES TEST I - MARK LIST	S	7 EEE- A	(2016-2	020 BAT	CH)			SEPTE	EMBEI	2019	,
_		OESECA	INDEX	EE401	EE403	EE405	EE407	EE409	EE469					
				EC	DGSG -	ESD	DSP	EMD	EHV	Total		NO OF		
SL No.	Roll No.	RANK	NAME	Feter Derus	Seay Kurina	Seethamma George	Discolumn F	Jane Maria S	Joseph M George		*	MO OF SUBJE CTS FAILE D	D/N	female
				60	60	60	60	60	60	360	-			
. 1	1	18	ABHUITH S	25	47	38	30	242	36	200	55.56	2	D	M
2	2	16	ABIN ANIL	39	49	32	31	3818	36	205	56.94	1	D	M
3	3	12	AGGY GEORGE	40	40	39	40	56	AB	215	59.72	0	LH	·F
4	4	3	AJAY M JOY	45	49	42	50	35	54	275	76.39	0	D	M
5	5	7	AKHIL BLJU	48	41	30	47	35	40	241	66.94	0	D	M
6	6	24	AKSHAY SIMON	39	40	30	182	18)	28	173	48.06	2	MH	M
7	7	19	ALEN MARTIN	39	40	36	31	27	26.	199	55.28	1	MH	M
8	8	14	AMMU JOVAN	36	39	42	41	27	29 .	214	59.44	0	D	F
9	9	22	ANAKHA RAJ	33	- 30	30	43	21	30	187	51.94	1	D	F
10	10	2	ANANDHU SELIVAN	50	49	42	59	46	55	301	83.61	0	D	M
11	11	11	ANUSREER	48	49	38	46	AB	40	221	61.39	0	LH	F
12	12	5	ARUN JANARDHANAN NAIR	43	48	44	43	35	39	252	70.00	0	MH	M
13	13	14	ATHULYA PETER	39	45	35	32	29	34	214	59.44	0	D	F
14	14	27	CHRISTY BABY	107	37	35	25	12.12	35	166	46.11	3	D	M
15	15	20	CIRIL KURIAN RISON	34	43	31	21	29	38	196	54.44	1	MH	M
16	16	1	DIPU JOSEPH VLIOY	52	49	56	50	57	46	310	86.11	0	D	M
17	17	. 25	DON DOMINIC	AB	48	32	26	27	38	171	47.50	1	D	M
18	18	10	FEBIN BIJU	39	49	37	40	28	31	224	62.22	0	D	M
19	19	26	JESWIN K ANTO	16	36	33	27	25	30	167	46.39	2	MH	M
20	20	28	JITHU THANKACHAN	220	45	36	31	22	AB	156	43.33	2	D	M
21	22	5	KRISHNANAND SAJI	45	42	42	49	32	42	252	70.00	0	D	M
22	23	29	K S NANDU KRISHNA	25	39	33	16	松15 基	24	152	42.22	4	D	M
23	24	34	MIDHUN SAJU	27	AB	AB	24	195	187	88	24.44	3	D	M
24	25	12	MOBIN KOSHY	34	48	40	33	33	27	215	59.72	0	MH	M
25	26	4	RUBEENA A A	48	43	34	55	36	41	257	71.39	0	D	F
2.6	27	33	SEBASTIAN SANOJ P	222	AB	AB	32	200	29	103	28.61	2	D	M
27	28	23	SOORAJ S SURESH	28	43	38	30	19	20	178	49.44	2	D	M
28	29	1.7	SREENATH S	36	39	33	265	29	38	201	55.83	1	D	M
29	30	9	SSANKARANARAYANAN	37	48	38	35	28	41	227	63.06	0	D	M
30	31	32	TANIL S KEERIKKATTU	28	AB	AB	30	1993	35	116	32.22	1	D	M
31	32	21	THOMAS IKE MATTHEW	34 .	36	34	42	27	22	195	54.17	1	D	M
32	33	8	VTMANOJ	43	36	32	42	54	27	234	65.00	0	D	M
33	34	31	SANJAY BABU V L	30	AB	13	33	10 19	2288	117	32.50	3	D	M
34	35	30	NOYALYV	24	34	23	100 m	169	22	133	36.94	5	D	M
	-	-	Average	35.30	42.70	35.42	35.06	28.67	33.53		-			
	-	240	Max.Mark	52	49	56	59	57	55					
	-	-	Min.Mark	16	30	13	14	15	18					
	-		No: of Full Pass	26	30	29	26	19	25					
			Pass Percentage	78.79	100.00	93.55	76.47	57.58	78.13					
	-		No: of All Pass		-	, ,,,,,,	10.47	-						
	_	Pe	ercentage of All Pass						1.12					
			Group Tutor : Oly	10/19							ноп	(EEE	0	



Established in 2001





VISWAJYOTHI COLLEGE OF ENGINEERING AND TECHNOLOGY , VAZHAKULAM

Department of Electronics & Communication Engineering WEAKER/BRIGHTER STUDENTS

Semester	<u> </u>
Batch	В
Assessment Year	2019-20

Subject	LINEAR ALGEBRA &
Course code	C 101
Faculty Name	DANY SEBASTIAN

Roll No	Name	Series 1	Series
KOII NO	Name	50	50
11	ADORN TYPACHEN	2.3	2.3
2	AJITH GEORGE LOUIS	21	13
3	AKSHAY SANKAR P	40	29
4	ALBIN SABU	37	30
5	ANITTA MAVIN	47	47
6	ANN MARIA VINOD	47	47
7	ANN MARY JAMES	50	42
8	ANTONY JOSE	33	40
9	APARNA BIJU	44	35
10	ARYA MANOHAR	22	23
11	ASHIK GEORGE	21	20
12	ASHLY JOSHY	25	33
13	ASIINA A A	21	30
14	BASIL BENNY	25	10
15	BENSON JOHN	24	15
16	BIJILA M ELDHO	15	16
17	BINUSREE P.A.	50	50
18	BIYNAKA MANI	34	20
19	BRIJIT SAJU	35	24
20	DEVIKA SUBASH	39	40
21	DINU JOY	35	39
22	EDWIN SIBY	31	19
23	FINU JAMES	40	24
24	IMRANKHAN A M	47	42
25	JIBIN JOY	37	24
26	JOE P B	41	37
27	JOYAL JOHNSON	48	41
28	JOYAL JOSE	46	48
29	KRISHNA S BIJU	16	32
30	LEON JOHNSON	31	23
31	MARIA REENA ROY	48	39
32	MEENU K R	7514	9
33	WICHAMINIAD BALTIAK	4 10	9
34	PRANAV PRADEEP	16	18
35	PEVATHY RAJEEVAN	49	47
	F DHAN BIJOY	36	28
37	SEMOL JOHN	33	24
38	S INDRA SANTY	30	32
	S EBIN JOSE	28	25
40	rownskoiii	44	8
41	NHOL YNCT	8	de 3 mm

Brighter Students Weaker Students

Dany Sebastian
Asst. Professor, S&H

Established in 2001 Managed by Catholic Diocese Kothamangalam



3. Participation certificates of students in various events

a) Techfest



Established in 2001 Managed by Catholic Diocese Kothamangalam







CERTIFICATE OF PARTICIPATION

THIS CERTIFICATE IS PRESENTED TO

ELIZABETH.V. VARGHESE

OF VICET

FOR PARTICIPATING IN SAIL BREAK

ON 29th FEBRUARY 2020 AT ADI SHANKARA INSTITUTE

OF ENGINEERING AND TECHNOLOGY, KALADY



Scanned with CamScanner

Established in 2001 Managed by Catholic Diocese Kothamangalam



b) Hackathon



Established in 2001







Established in 2001 Managed by Catholic Diocese Kothamangalam

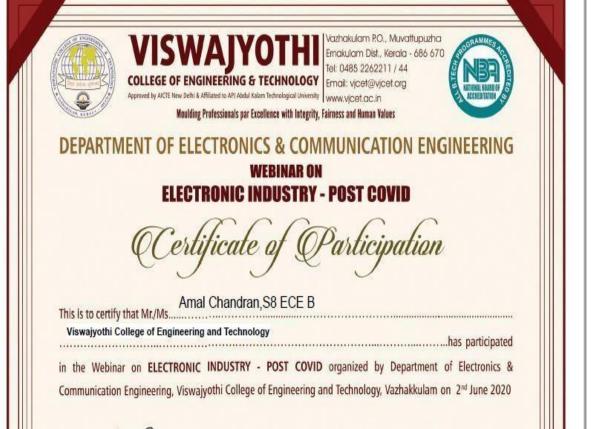


c) Webinar



Established in 2001 Managed by Catholic Diocese Kothamangalam





Established in 2001 Managed by Catholic Diocese Kothamangalam



d) Workshop



This certificate is proudly presented to

BINDU VINCENT

on successful completion of the **PCB Designing** workshop held at Viswajyothi College of Engineering and Technology, Vazhakulam on 9th and 10th August 2019.







Established in 2001 Managed by Catholic Diocese Kothamangalam





TO WHOM IT MAY CONCERN

Spec/Koc/Data_Science_Workshop/10/2019

18th Oct 2019

SUB: Data Science Workshop Participation Certificate

This is to certify that ALEENA SARA BABY had participated in the DATA SCIENCE WORKSHOP conducted by SPECTRUM SOFTTECH SOLUTIONS (P) LTD. on 16th Oct 2019.

SPECTRUM (www.spectrum.net.in) is a private IT Park located at Mahakavi G. Road, Kochi-11, Kerala, India, offering a range of IT & IT-Enabled Services to a host of clients in INDIA and USA. We conduct workshops, seminars, and internships to equip technology professionals and career aspirants to face the challenges in changing/upcoming technologies.

We wish this participant all success.

Yours truly,

JOSEPH JOB | Chief Technology Officer

Spectrum Softtech Solutions Pvt. Ltd.



Established in 2001 Managed by Catholic Diocese Kothamangalam











Certificate of Participation

Awarded to

Tony Kurian

of

VJCET vazhakulam

for attending the workshop on "Arduino Programming" organized by IEEE PES and IEEE WIE AG of Viswajyothi College of Engineering and Technology in May 2020.

Uthara Pradeep

Chair IEEE PES, VJCET Katherin Jose

Chair IEEE WIE AG, VJCET Anish M Jose

Counselor IEEE Student Branch, VJCET

Established in 2001 Managed by Catholic Diocese Kothamangalam



e) Conferences



Established in 2001 Managed by Catholic Diocese Kothamangalam





VISWAJYOTHI

COLLEGE OF ENGINEERING & TECHNOLOGY Email: vjcet@vjcet.org

Vazhakulam RO., Muvattupuzha Ernakulam Dist., Kerala - 686 670 Tel: 0485 2262211 / 44 Ernall: vjcet@vjcet.org



Moulding Professionals par Excellence with Integrity, Fairness and Human Values

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

12™ NATIONAL CONFERENCE ON VLSI, SIGNAL PROCESSING AND COMMUNICATION VLES '20

Certificate of Participation

This is to certify that Mr./Ms./Dr. ANU MARIA SUNNY, S8 ECE B

has presented a paper titled. AUDIO SPOTLIGHTING

in VLES'20, NATIONAL CONFERENCE ON VLSI, SIGNAL PROCESSING AND COMMUNICATION organized by Department of Electronics & Communication Engineering, Viswajyothi College of Engineering and Technology, Vazhakkulam on 14th & 15th July 2020

Mrs. Smitha Cyriac HOD Dr. K.K.Rajan Principal

Established in 2001



f) **Online Courses**

This certificate is computer generated and can be verified by scanning the QR code given below. This will display the certificate from the NPTEL repository, https://nptel.ac.in/noc/

Roll No: NPTEL20CS15S1380564

ALAN SHAJU EDASSERIL HOUSE, ROCHKULAM P.O TURNINGSHA



No. of credits recommended by NPTEL:2

is it fit, hased on the actual student effort involved





This certificate is awarded to

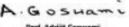
ALAN SHAJU

for passing the course



with Score* 87 %

Jan-Mar 2020 (8 week course)



Prof. Adrijit Goswami



Indian Institute of Technology Kharagpur

Continuous online assessment score

To validate and check scores: http

Established in 2001 Managed by Catholic Diocese Kothamangalam





(Funded by the Ministry of HRD, Govt. of India)





This certificate is awarded to

ALAN BINOY

for successfully completing the course

Manufacturing of Composites

with a consolidated score of

Online Assignments 24.58/25 Proctored Exam 60/75

Chairman, Centre for Continuing Education

Total number of candidates certified in this course: 843

Aug-Oct 2019 (8 week course)



Indian Institute of Technology Kanpur

Roll No: NPTEL19ME67S51300224

To validate and check scores: https://nptel.ac.in/noc

Established in 2001 Managed by Catholic Diocese Kothamangalam





Established in 2001 Managed by Catholic Diocese Kothamangalam



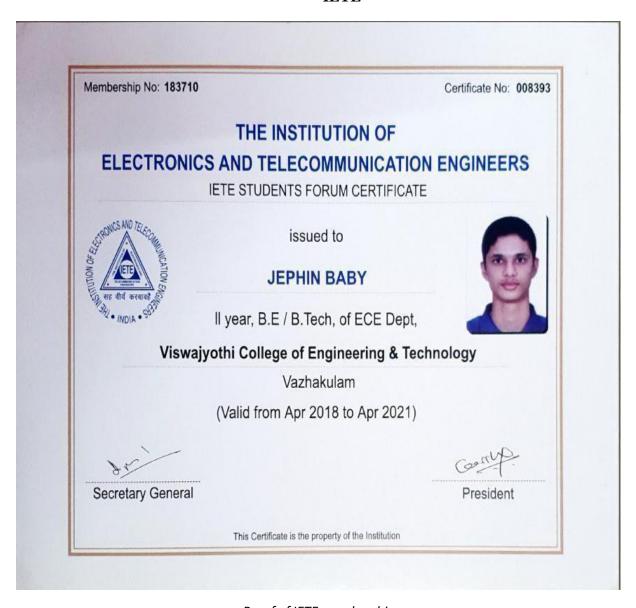


Established in 2001 Managed by Catholic Diocese Kothamangalam



4. Student membership in professional Body

IETE



Proof of IETE membership

Established in 2001 Managed by Catholic Diocese Kothamangalam





The Institution of Electronics and Telecommunication Engineers

KOCHI CENTRE

3rd Floor, Jewel Arcade, Layam Road, Kochi-682 011 Telefax: (+)91-484-2369944 E-mail: kochi lete@gmail.com, letekochi@dataorie.in Website: www.ietekochi.org

IETE/KOCHI/WTISD/001/2019

Dated: 18th May 2019

Certificate of Participation

This is to certify that Mr. Jephin Baby, Viswajyothi College of Engineering & Technology, Vazhakulam has actively participated in the one day programme organized by IETE Kochi Centre on 17^h May 2019 on the occasion of the "World Telecommunication and Information Society Day".

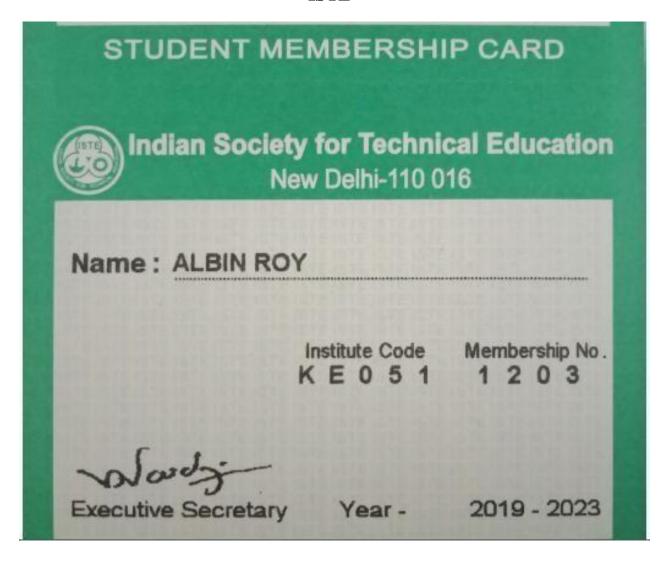


C. Krishnakumar Hon. Secretary

Established in 2001 Managed by Catholic Diocese Kothamangalam



ISTE



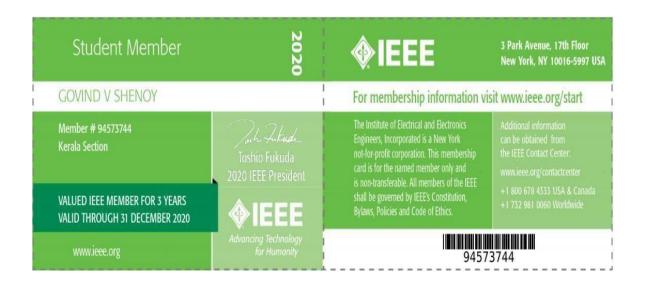
Proof of ISTE membership

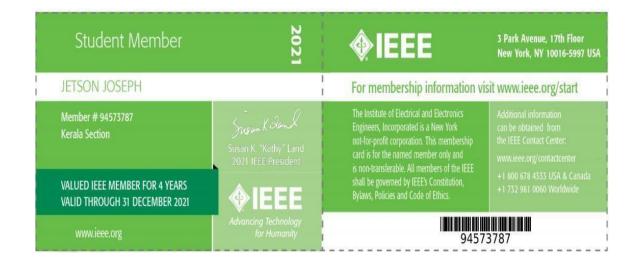


Established in 2001 Managed by Catholic Diocese Kothamangalam



IEEE





Established in 2001







Established in 2001





Established in 2001 Managed by Catholic Diocese Kothamangalam



CSI



CSI ACCREDITED STUDENT

Name: Devika Suresh Kumar

ID No: 01462053

Valid till: 30th June 2021

Viswajyothi College of Engineering and Technology

Vazhakulam Post, Muvattupuzha, Ernakulam - 686670,

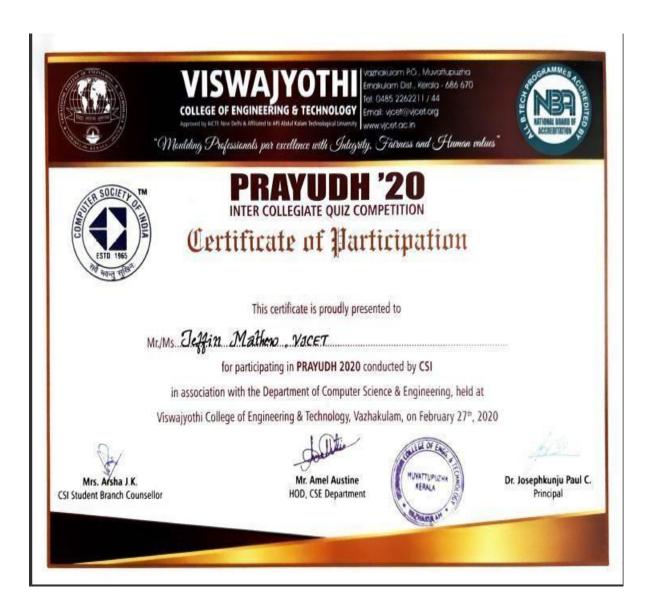
Kerala.

Hon. Secretary

Proof of CSI membership

Established in 2001 Managed by Catholic Diocese Kothamangalam





Established in 2001 Managed by Catholic Diocese Kothamangalam



5. Gate Coaching



Gate coaching Attendence list of 2016-2020 ECE batch

SL NO.	NAME	11/10/2018	11/11/2018	11/18/2018	11/20/2018	11/25/2018
1	VISHNU M	A	A		P	Р
2	SNEHA SUNNY .	P	р		P	P
3	MERIN THOMAS	A	P		P	P
4	JEPHIN BABY	A	P	HOLIDAY	P	P
5	ANU MARIA SUNNY	Р	P		P	P
6	SHARON ALICE	P	. Р	1	Α	A
7	MERLIN JOHNSON	Р	P	1 1	P	P
	FACULTY NAME	DEEPTHI	DEEPTHI	NO	ROSMIN	MERIN
	SUBJECT	SAS	SAS	NO	DIGITAL	NETWORK

Gate coaching Attendence list of 2016-2020 CE batch

SL NO.	NAME	11/10/2018	11/11/2018	11/18/2018	11/20/2018	11/25/201
1	ANNMARY VINCENT	P	P		Р	P
2	AVANI MOHAN	Р	Р	1	Р	A
3	REVATHY G KARTHA	Р	P	1	Р	P
4	ASHMY YOOSEPH	Р	P		P	р
5	RINCY JOHNY	Р	Р		P	P
6	ANJANA JAYAKUMAR	Р	P	HOLIDAY	P	P
7	ANITTA THOMAS	A	P	1	Р.	p
8	THOMAS V SANTHOSH	Р	P	1	P	р
9	ALBIN SUNNY	Р	. Р		P	p
10	DIYA GEORGE	Р	Р		Р	P
	FACULTY NAME	ANITH	NIMISHA	NO CLASS	JERRY(PF)	ANITH
	SUBJECT	FM	MOS	NO CLASS	G MECHANICS	FM

Gate coaching Attendence list of 2016-2020 ME batch

SL NO.	NAME	10/11/2018	11/11/2018	11/18/2018	11/20/2018	11/25/2018
1	ABEX MAVIN	P	P		Р	р
	FACULTY NAME	ANITH	NIMISHA	HOLIDAY	JERRY(PF)	ANITH
	SUBJECT	FM	MOS	ENGG MECHANICS(6		FM

Mr.C. Mavin

AP & PO



Established in 2001 Managed by Catholic Diocese Kothamangalam





OFFICE OF THE COMMISSIONER FOR ENTRANCE EXAMINATIONS, KERALA

KMAT KERALA 2020

ENTRANCE EXAMINATION FOR ADMISSION TO MBA COURSE - 2020

SCORE CARD

Communication Address		A-129, KUREEKAD CHOTTA akulam, Kerala, 682305	NIKARA,	Amuitha
Name of Candidate	AMRITHA SATHE	ESH KUMAR		
Roll Number	73290	Application No.	6103436	
Date of Entrance Examination	21-06-2020	Declaration of Result	27-07-2020	

	Subjects	Score Obtained	Maximum Score
1	English Language Usage and Reading Comprehension	62	200
11	Quantitative Aptitude	78	200
Ш	Data Sufficiency and Logical Reasoning	18	160
IV	General Knowledge and Current Affairs	16	160
	Total	174	720

In accordance with the minimum eligibility criteria for admission to MBA course as mentioned in the information Bulletin for KMAT-2020, the cut off scores for various categories are as follows:

Category	Minimum Eligibility Percentage	Cut-off Score(Out of 720)
General Category	15%	108
SEBC Category	10%	72
SC/ST Category	7.5%	54

Place: Thiruvananthapuram

Date: 28-07-2020



Commissioner for Entrance Examinations

Printed on 28-07-2020 19:47:31 IP:157.44.141.131

Proof of competitive exam participation

Established in 2001 Managed by Catholic Diocese Kothamangalam





Test Taker Score Report

Name: ELDOSE, MIDHUN

Last (Family/Sumame) Name, First (Given) Name Middle Name

Email: meldose@gmail.com

Gender: M

Appointment Number: 3445 1092 0218 1255

Date of Birth: April 15, 1998 Test Date: April 17, 2020

ELDOSE, MIDHUN Navullil house v k colony P O Thevakkal ,kerala Thevakkal,Kerala kochi-21 Ernakulam, Kerala 682021 India



Inst. Code Dept. Code

Country of Birth: India Native Language: Malayalam

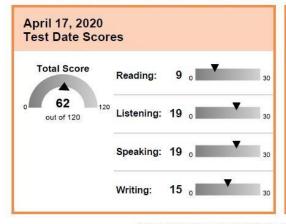
Test Center: STNRPIND - Special Home Edition

Test Center Country: India

Security Identification

ID Type: PASSPORT ID No.: xxxxxxxxxxxxxxxxxx7739 Issuing Country: India

THIS IS A PDF SCORE REPORT, DOWNLOADED AND PRINTED BY THE TEST TAKER.





A total score is not reported when one or more sections have not been administered. Expired scores are not included in MyBest™ calculations.

86-86

Copyright © 2019 by Educational Testing Service. All rights reserved. ETS, the ETS logo, TOEFL and TOEFL iBT are registered trademarks of Educational Testing Service (ETS) in the United States and other countries. MyBest is a trademark of ETS.

Established in 2001 Managed by Catholic Diocese Kothamangalam





Test Taker Score Report

THIS IS A PDF SCORE REPORT, DOWNLOADED AND PRINTED BY THE TEST TAKER.

ELDOSE, MIDHUN

Date of Birth: April 15, 1998

Appointment Number: 3445 1092 0218 1255 Test Date: April 17, 2020

SCORE RANGES

Total Score	0-120
Reading	0-30
Advanced	24-30
High - Intermediate	18-23
Low - Intermediate	4-17
Below Low - Intermediate	0-3
Listening	0-30
Advanced	22-30
High - Intermediate	17-21
Low - Intermediate	9-16
Below Low - Intermediate	0-8
Speaking	0-30
Advanced	25-30
High - Intermediate	20-24
Low - Intermediate	16-19
Basic	10-15
Below Basic	0–9
Writing	0-30
Advanced	24-30
High - Intermediate	17-23
Low - Intermediate	13-16
Basic	7-12
Below Basic	0-6

INSTITUTION CODES

The Institutions and Department code numbers shown on the front page are the ones you selected before you took the test.

Dept.	Where the Report Was Sent
00	Admissions office for undergraduate study
01, 04-41, 43-98	Admissions office for graduate study in a field other than management (business) or law according to the codes selected when you registered
02	Admissions office of a graduate school of management (business)
03	Admissions office of a graduate school of law
42	Admissions office of a school of medicine or nursing or licensing agency
99	Institution or agency that is not a college or university

For additional information about TOEFL iBT scores, score ranges, and how to improve your skills, visit www.ets.org/toefl/ibt/scores.

IMPORTANT NOTE TO SCORE USERS: This is a PDF score report, downloaded and printed by the test taker. Therefore, ETS cannot guarantee that it has not been altered. To verify the scores on this report, please contact the TOEFL Score Verification Service at +1-800-257-9547 or +1-609-771-7100. Scores more than two years old cannot be reported or validated.

Copyright © 2019 by Educational Testing Service. All rights reserved. ETS, the ETS logo, TOEFL and TOEFL iBT are registered trademarks of Educational Testing Service (ETS) in the United States and other countries. MyBest is a trademark of ETS.

Proof of competitive exam participation

Established in 2001 Managed by Catholic Diocese Kothamangalam



6. Funded Projects



Kerala State Council for Science, Technology and Environment

Prof (Dr.) K.P. Sudheer Executive Vice President KSCSTE, Pattom

16.01.2020

Letter No. 01056 /SPS 64/2019/KSCSTE

Dear Mr. Cyriac M Odackal.

Sub:-Financial assistance for Student Project scheme of KSCSTE reg. Ref:-Your application received under Student Project scheme

This is to invite your attention to the reference cited and to inform that the project proposal titled "Stroke Rehab and Exercising Glove" submitted by Mr. Cyriac M Odackal as PI and Jephin Baby, Vishnu M,Amal Chandran as student investigator(s) has been approved. An amount of \$10000/- is sanctioned by the Council. The budget estimate of the project is as detailed below.

SL.NO.	ITEMS	
1	Consumables	AMOUNT(₹)
2	Minor equipments	7500
3	Travel	1000
4		500
5	Research Literature & Documentation	500
3	Others (for analysis)	500
	Total	10000

The PI has to submit the signed Terms and Conditions (as per the guidelines) and the date of start of the project within two weeks to the undersigned. The project should be completed within six months and submit the certified soft copy of the final report (in pdf to sed.kscste@kerala.gov.in), audited Statement of Expenditure and Utilization Certificate counter signed by the Head of the Institution for releasing the grant. The format for final report, SE and UC can be downloaded from www.kscste.kerala.gov.in.

Thanking you,

Yours sincerely,



To

Prof (Dr.) K.P. Sudheer

Mr. Cyriac M Odackal, Associate Professor, Dept. of Electronics & Communication, Viswajyothi College Of Engineering And Technology, Vazhakulam P.O, Muvattupuzha, 686670

Copy to:

The Principal, Viswajyothi College Of Engineering And Technology, Vazhakulam P.O, Muvattupuzha, 686670

Jephin Baby, Vishnu M, Amal Chandran, Student(s), Bachelor of Technology (BTech), Electronics & Communication, Viswajyothi College Of Engineering And Technology, Vazhakulam P.O, Muvattupuzha, 686670

Sasthra Bhavan, Pattom P.O., Thiruvananthapuram - 695 004, Kerala State, India Tel : 0471 - 2548200-09, EVP - 2543557, 2548222, MS - 2534605, 2548220, CoA - 2543556, 2548248 Fax: 0471 - 2540085, 2534605 e-mail: kscste@gmail.com, www.kscste.kerala.gov.in

Scanned by CamScanner

Established in 2001 Managed by Catholic Diocese Kothamangalam





Kerala State Council for Science, Technology and Environment

Prof (Dr.) K.P. Sudheer Executive Vice President KSCSTE, Pattom 16.01.2020

Letter No. 00344 /SPS 64/2019/KSCSTE

Dear Mr. Eldhose Kurian,

Sub:-Financial assistance for Student Project scheme of KSCSTE reg. Ref:-Your application received under Student Project scheme

This is to invite your attention to the reference cited and to inform that the project proposal titled "PORTABLE NUTMEG SEPARATOR-NUX" submitted by Mr. Eldhose Kurian as PI and Eldhose Raju,Albin Paul,Harikirishnan A S. Jijiil P. Chettoor as student investigator(s) has been approved. An amount of \$10000/ is sanctioned by the Council. The budget estimate of the project is as detailed below.

SL.NO.	ITEMS	AMOUNT(₹)
1	Consumables	7565
2	Minor equipments	435
3	Travel	1050
4	Research Literature & Documentation	500
5	Others (for analysis)	450
	Total	10000

The PI has to submit the signed Terms and Conditions (as per the guidelines) and the date of start of the project within two weeks to the undersigned. The project should be completed within six months and submit the certified soft copy of the final report (in pdf to sed-kscste@kerala.gov.in), audited Statement of Expenditure and Utilization Certificate counter signed by the Head of the Institution for releasing the grant. The format for final report, SE and UC can be downloaded from www.kscste.kerala.gov.in (

Thanking you,

Yours sincerely,



Prof (Dr.) K.P. Sudheer

To

Mr. Eldhose Kurian, Assistant Professor, Dept. of Mechanical Engineering, Viswajyothi College Of Engineering And Technology, Vazhakulam P.O, Muvattupuzha, 686670

Copy to:

The Principal, Viswajyothi College Of Engineering And Technology, Vazhakulam P.O, Muvattupuzha, 686670

Eldhose Raju, Albin Paul, Harikrishnan A S, Jipil P Chettoor, Student(s), Bachelor of Technology (BTech), Mechanical Engineering, Viswajyothi College Of Engineering And Technology, Vazhakulam P.O, Muvattupuzha, 686670

Sasthra Bhavan, Pattom P.O., Thiruvananthapuram - 695 004, Kerala State, India Tel: 0471 - 2548200-09, EVP - 2543557, 2548222, MS - 2534605, 2548220, CoA - 2543556, 2548248 Fax: 0471 - 2540085, 2534605 e-mail: kscste@gmail.com, www.kscste.kerala.gov.in

Scanned with CamScanner

Established in 2001



7. Best outgoing student

Total Marks till S7		40	Criteria for BEST OUTGOING STUDENT						
Placement		10							
GATE, MAT, CAT,	, GMAT etc	10							
			Achievements	10	2 marks for each event. Will consider only 1,2 & 3 positions. Maximum of 5 events. In Paper presentation and project presentation, for participation 1 mark for each event. Max. of 5 events. Limited to 10 marks.				
Extra Curricular Activities	Technical	20	Professional Body Membership	5	2 marks for each membership. Limited to 5 marks.				
			Leadership	5	2marks for each event: Limited to 5 marks. (Only for coordinators & not for committee member)				
		5576	Achievements	10	College level - 1 mark for each event, University Level - 2 marks for each event, State Level - 3 marks for each event, National Level - 4 marks for each event. Max, marks limited upto 10marks.				
	Non Technical	n Technical 20	Leadership	10	Union executive members - 5 marks Team member (Lollege Learn) - 1 mark for one type of team. Limited to a max. of 5 marks 2 marks for each event. Limited to 5 marks. (Only for coordinators & not for committee member). Max. marks limited upto 10 marks.				
То	tal	100							
					MUNITUPURNA PRINCIPAL				



Established in 2001







Short listed students for best outgoing student of the year 2019-2020

Department	Name of the student	Mark(100)
Department of Mechanical Engineering	Eldhose Raju	96.3
Department of Electronics & Communication Engineering	Megha Sukumar	80
Department of Computer Science & Engineering	Jintu Justin	71.52
Department of Electrical & Electronics Engineering	Aparna R Nair	65.24
Department of Civil Engineering	Anjana Jayakumar	57
Department of Information Technology	Binitta Thomas	37





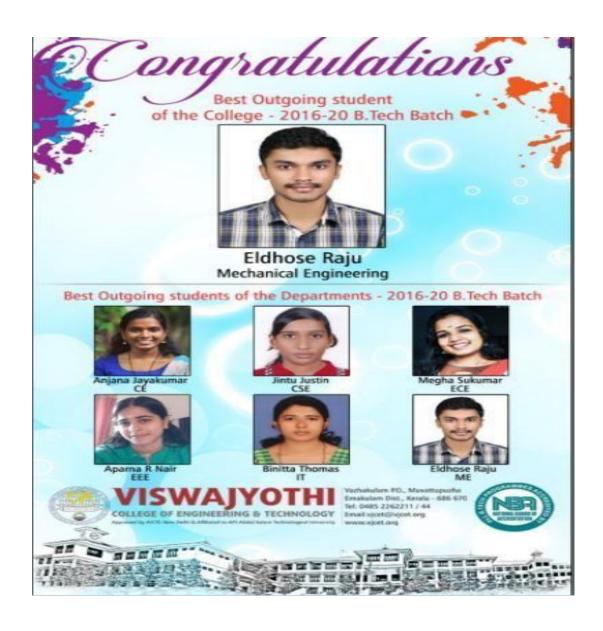
PRINCIPAL





Eldhose Raju(2016-2020) receives best outgoing student award





Established in 2001



VISWAJYOT





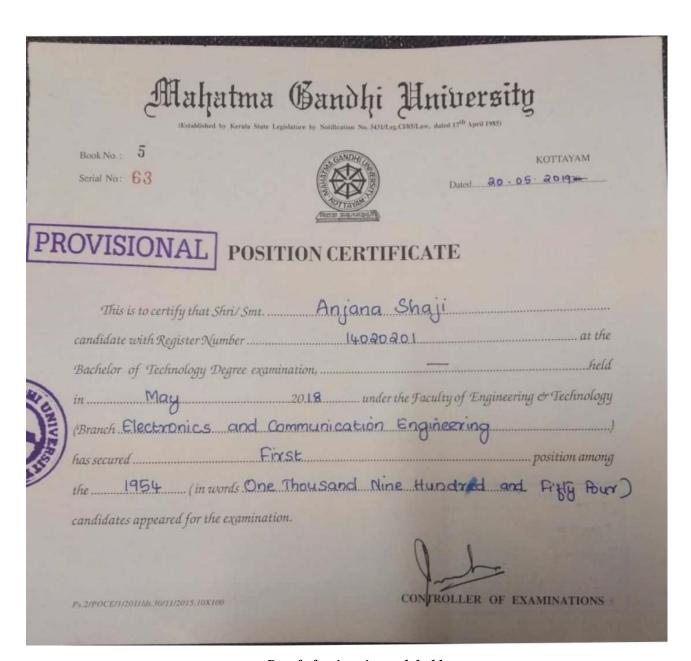
Proficiency Award 2016-2020 batch - topper from each branch(upto 7th semester)

Department	Name of the student	CGPA
Department of Mechanical Engineering	Johns Varghese G	9.45
Department of Computer Science & Engineering	Jintu Justin	9.13
Department of Electrical & Electronics Engineering	Nandhukrishna B	9.24
Department of Electronics & Communication Engineering	Merin Thomas	9.27
Department of Civil Engineering	Anjana Jayakumar	9.33
Department of Information Technology	Binitta Thomas	8.71



Established in 2001 Managed by Catholic Diocese Kothamangalam





Proof of university rank holder

Established in 2001

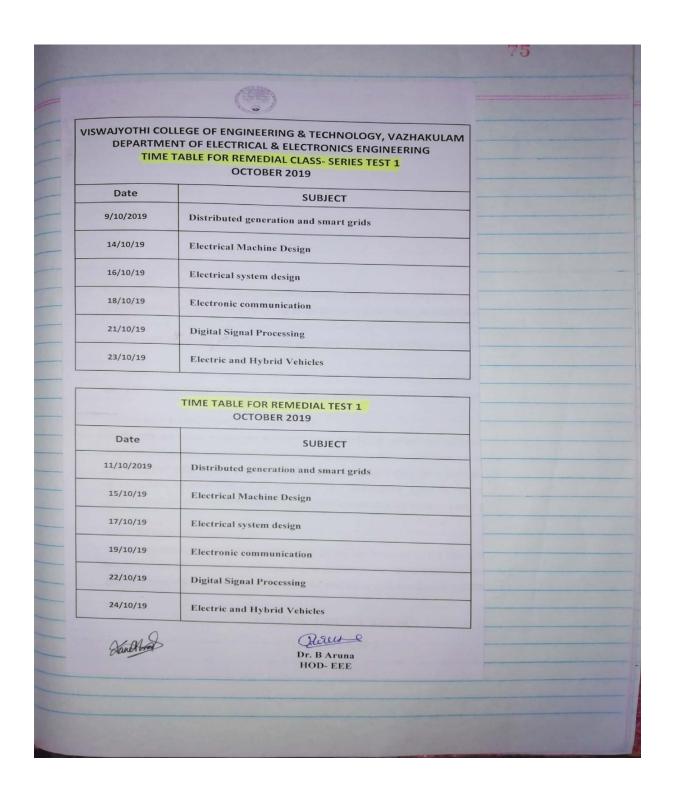


8. Remedial class

-			VISWAJYOTHI COLL DEPARTMEN	TOFEL	ECTRIC	CAL AND		RONICS			IAKUL	AM		
		SERI	ES TEST I - MARK LIST								SEPTE	EMBE	R 2019	9
		G.L.	INDEX	EE401	EE403	EE405	EE407	EE409	EE469					
				EC	DGSG -	ESD	DSP	EMD	EHV	Total		NO OF		
SL No.	Roll No.	RANK	NAME	Jibby Feter Derus	Sony Kurima	Seethamata George	Dilecphanna r P	Jane Maria S	Joseph M George		~	MO OF SUBJE CTS FAILE D	D/M	female
				60	60	60	60	60	60	360		-	-	
1	1	18	ABHIJITH S	25	47	38	30	24	36	200	55.56	1	D	M
2	2	16	ABIN ANIL	39	49	32	31	2018	36	205	56.94		D	M
3	3	12	AGGY GEORGE	40	40	39	40	56	AB	215	59.72	0	LH	1000
4	4	3	AJAY M JOY	45	49	42	50	35	54	275	76.39 66.94		D	M
5	5	7	AKHIL BLJU	48	41	30	47	35	28			0	D	M
6	6	24	AKSHAY SIMON	39	40	30	1828	18	THE PERSON NAMED IN	173	48.06	2	MH	M
7	7	19	ALEN MARTIN	39	40	36	31	27	26	214	59.44	0	MH	.M
8	8	14	AMMU JOVAN	36	39	30	41	27	30	187	51 94	1	D	F
9	10	22	ANAKHA RAJ ANANDHU SELIVAN	50	49	42	59	46	55	301	83.61	0	D	M
10	11	11	ANANDHU SELIVAN ANUSREE R	48	49	38	46	AR	40	221	61.39	0	LH	F
12	12	5	ARUN JANARDHANAN NAIR	48	49	44	43	35	39	252	70.00	0	MH	M
13	13	14	ATHULYA PETER	39	45	35	32	29	34	214	59.44	0	D	F
14	14	27	CHRISTY BABY	A DAME	37	35	225	112	35	166	46.11	3	D	M
15	15	20	CIRIL KURIAN RISON	34	43	31	2)1	29	38	196	54.44	1	MH	M
16	16	1	DIPU JOSEPH VLIOY	52	49	56	50	57	46	310	86.11	0	D	M
17	17	25	DON DOMINIC	AB	48	32	26	27	38	171	47.50	1	D	MI
18	18	10	FEBIN BIJU	39	49	37	40	28	31	224	62.22	0	D	M
19	19	26	JESWIN K ANTO	1000	36	33	27	10025111	30	167	46.39	2	MH	M
20	20	28	JITHU THANKACHAN	22	45	36	31		AB	156	43.33	2	D	84
21	22	5	KRISHNANAND SAJI	45	42	42	49	32	42	252	70.00	0	D	M
22	23	29	K S NANDU KRISHNA	8625 E	39	33	162	8215 kg	2000 A 1000	152	42.22	4	D	M
23	24	34	MIDHUN SAJU	27	AB	AB	24	4 1939	98181	88	24.44	3	D	M
24	25	12	MOBIN KOSHY	34	48	40	33	33	27	215	59.72	0	MH	M
25	26	4	RUBEENA A A	48	43	34	55	36	41	257	71.39	0	D	F
26	27	33	SEBASTIAN SANOJ P	222	AB	AB	32	20第	29	103	28.61	2	D	M
27	28	23	SOORAJ S SURESH	28	43	38	30	19	20	178	49.44	2	D	M
28	29	17	SREENATH S	36	39	33	26	29	38	201	55.83	1	Đ	NE
29	30	9	SSANKARANARAYANAN	37	48	38	35	28	41	227	63.06	0	D	M
30	31	32	TANIL S KEERIKKATTU	28	AB	AB	30	福約230 图	35	116	32.22	1	D	NE
31	32	21	THOMAS IKE MATTHEW	34 .	36	34	42	2.7	22	195	54.17	1	D	N1
33	33	8	LONAMIA	4.3	36	32	42	54	27	234	65.00	0	D	M
33	34	31	SANJAY BABU V L	30	AB	13	33	19	18 22 E	117	32.50	3	D	M
34	35	30	NOYAL V V	24	34	23	13	169	22	133	36.94	5	D	M
			Average	35.30	42.70	35.42	35.06	28.67	33.53					
		-	Max.Mark	52	49	56	59	57	55					
			Min.Mark	16	30	13	14	15	18					
			No: of Full Pass	26	30	29	26	19	25					
			Pass Percentage	78.79	100.00	93.55	76.47	57.58	78.13					
			No: of All Pass					-	15					
		-	Group Tutor	2019				44	.12		(Se	CEER An	0	-

Established in 2001 Managed by Catholic Diocese Kothamangalam







Subject :	Ele	etric and Hybrid Vehicles		a 112/10		
Staff ;	: 3	Ar. JOMU M GEORGE	Topic	Types hybrid	Test	
Criteria :	The	se who failed in Series Test I (less than 45% marks)		of developmen		
SI No.	Roll No.	- 20100	Deration	4.19 - 5 pm		
1		Name A/ A/ F	Date	23/10/19	24/00/19	
_	7	Alen Martin		-		
2	23	K-S Namde	deesha			
3	24	Midhun So	nju			
4	100		Ruesh	X	×	AHO
5	32	Thomas 1k	e Mathews	×	×'	1 /W
6	34	The second secon	on VL	×	X	
7	35	Noyal V U	7	X	×	
3						V

Established in 2001



VISWAJYOTHI COLLEGE OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRONICS AND COMMUNICATION TIME TABLE - SI ECE A& B

REMEDIAL CLASS FOR SERIES TEST 1

SUBJECT DATE LINEAR ALGEBRA & CALCULUS 14/10/2019 ENGINEERING CHEMISTRY 15/10/2019 ENGINEERING GRAPHICS 16/10/2019 BASICS OF CIVIL ENGINEERING 17/10/2019 BASICS OF MECHANICAL 18/10/2019 **ENGINEERING**

REMEDIAL TEST FOR SERIES TEST 1

DATE	SUBJECT
21/10/2019	LINEAR ALGEBRA & CALCULUS
22/10/2020	ENGINEERING CHEMISTRY
23/10/2021	ENGINEERING GRAPHICS
24/10/2022	BASICS OF CIVIL ENGINEERING
25/10/2023	BASICS OF MECHANICAL ENGINEERING

Group Tutors:

Sani John (S1 ECA) Merlin Thomas (S1 ECB)





Subject: Linear Algebra Bo Calculus

No Date Name 9	(stude 5)	Sign To
Viswajyothi College of Engin	eering and Technolog	y, Vazhakulam
Department of S	Science and Humanitie	25
	Class Attendance	
inss: S1 ECB Subject: iculty in Charge: ဤ ຄາຊ ເພື່ອນຕົ້ນງ	Linuar Again & Co Date: 14-10-201	dedin 9
Not Name	(Bignature	Topics Handled
1 Benson John	500	
I Tony Jenn	Tour	
3 Pronew Pradeep	82	
4. Bijila M Eldho	Rigida	-24
5 Kirghan C. Bris	9663	3
6. Meener, b. R.	The same	- Fourier
1 Muhammar Lafthar	GI-F.	Series
& Thomashabby Terrient	China Control	
		_
		-
		-
aculty in Charge		Mic

Established in 2001



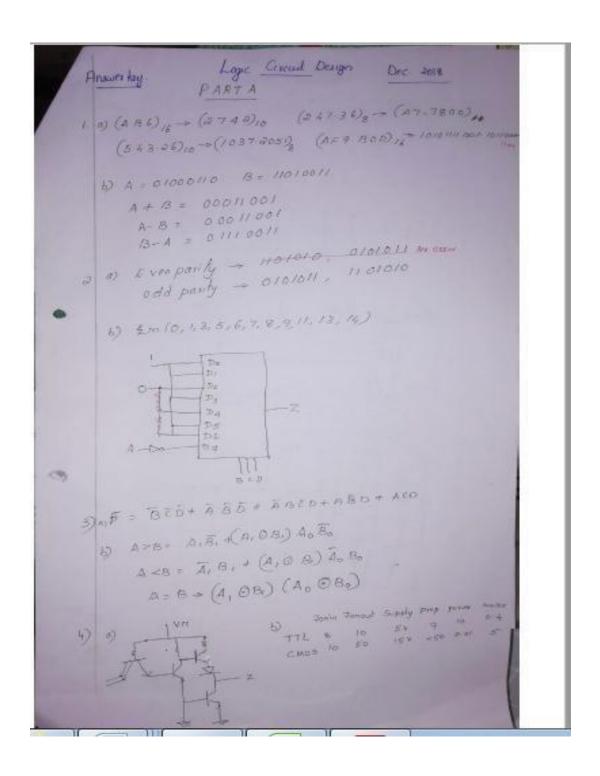
9. University Question paper and Answer Key

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY THIRD SEMENTER R.TECH DEGREE EXAMINATION. DECEMBER 2018 Course Code; EC207 Course Name: LOGIC CIRCUIT DESIGN (EC, AE) Mrs. Marks: 100 PART A Arrance any two full questions, each corries 15 marks. (8) (AB6) ₁₀ to Decimal (ii) (543.26) ₁₁ into Octal (iii) (247.35) ₂ into Hexa Decimal (iii) (AF9.BOD) ₁₀ into Binney b) Consider the agned bissary numbers A = 01000110 and B = (1010011 where B is in 2°s complement form, Find the value of the following mathematical expression (i) A+B (ii) B-A 2 a) Hamming code was used to generate parity for a nibble. If received bit sequence is 0101010 then write correct bit sequence with (i) Even parity (ii) Odd parity b) Explain the operation of a 8x1 multipleaver and implement the following using (7) an 8x1 multipleaver F(A, B, C, D) = \(\superatorname{O}\) (0, 3, 5, 5, 7, 8, 9, 11, 13, 14) 3 Minemize the following logic function using K- maps and realize using NAND gates alone F(A, B, C, D) = \(\superatorname{O}\) (0, 5, 8, 9, 11, 15) + d (2, 5) b) Design a magnitude comparator to compare two 2-bit mathbers A = A ₁ A ₀ and C) B = B ₁ B ₁ PART B Answer any two full questions, each carriers 15 marks. 4 a) Draw the current and explain the operation of TTI, NAND gate b) Compare TTL, CMOS logic families in terms of fan-in, fam-out, supply voltage, propagation delay, power dissipation and noise margin 5 a) Implement the following function using PLA F1(x, y, x) = \(\superatorname{O}\) (0, 1, 6, 7) Page 1 of 2	E	R3958 Pages:	
THERD SEMESTER RECHIDESCREE EXAMINATION, DECEMBER 2018 Course Code; #C207 Course Name: LOGIC CIRCUIT DESIGN (EC, AF) Duration: 3 Hours Max. Marks: 100 PART A Answer out two full questions, each corries 15 marks. (8) (1) (AB6) ₁₀ to Decimal (ii) (\$43,26) ₁₂ into Octal (ii) (47,35) ₁₅ into Hexa Decimal (iv) (AF9,B0D) ₁₀ into Binny b) Consider the agned binny numbers A = ## ## ## ## ## ## ## ## ## ## ## ## #	Reg	n. Name:	
Course Name: LOGIC CIRCUIT DESIGN (EC, AE) Max. Marks: 100 PART A Answer any two full questions, each corries 15 marks. Answer any two full questions, each corries 15 marks. (a) Consert the following (ii) (AB6) _{in} to Decimal (iii) (545,26) ₁₀ into Octal (iii) (247,38) ₆ into Hexa Decimal (iv) (AF9,BOD) ₁₀ into Octal (iii) (247,38) ₆ into Hexa Decimal (iv) (AF9,BOD) ₁₀ into Binney b) Consider the signed binary numbers A = 01000150 and B = 11010011 where B is in 2's complement form, Find the value of the Informing mathematical expression (1) A+B (iii) B-A 2 a) Hamming code was used to generate parity for a nibble. If received bit sequence is 0101010 then write correct bit sequence with (i) Exen parity (ii) Odd parity b) Explain the operation of a 8x1 multiplexer and implement the following using an 8x1 multiplexer F(A, B, C, D) = \(\Sigma \text{(0, 3, 3, 5, 6, 7, 8, 9, 11, 13, 14)} \) 3 Minimize the following logic function using K- maps and realize using NAND (10) gates alone F(A, B, C, D) = \(\Sigma \text{(0, 3, 5, 8, 9, 11, 15)} + d (2, 5) \) b) Design a magnitude comparation to compare two 2-bit mambers A = A ₁ A ₀ and (5) B = B ₁ B ₁ Answer any two full questions, each carries 15 marks. 4 a) Draw the current and explain the operation of TTL NAND gate b) Compare TTL, CMOS logic families in terms of famin, fam-ost, supply voltage, propagation delay, power dissipation and noise margin a) Implement the following function using PLA F(X, y, z) = \(\Sigma \text{(1, 1, 2, 4, 6)} \) F2xx, y, z) = \(\Sigma \text{(1, 1, 6, 7)} \)	10000		
Max. Market 100 PART A Answer any two full questions, each corrier 15 marks, (8) (1) (AB6), to Decemal (iii) (\$43,26); into Octal (iii) (247,56); into Decemal (iv) (AF9,B0D)); into Decimal (iv) (AF9,B0D)); into Binney b) Consider the signed binary numbers A = 01000110 and B = 11010011 where B is in 2% completion form, Fand the value of the following mathematical expression (i) A+B (ii) B-A 2 a) Hamming code was used to generate parity for a nibble. If received bit sequence is 0101010 then write correct bit sequence with (i) Exen parity (ii) Oxid parity h) Explain the operation of a 8x1 multiplexer and implement the following using an 8x1 multiplexer F(A, B, C, D) = \(\subseteq \text{m} (0, 3, 3, 5, 6, 7, 8, 9, 11, 13, 14) 3 Minimize the following logic function using K- maps and realize using NAND (10) gates alone F(A, B, C, D) = \(\subseteq \text{m} (0, 3, 5, 8, 9, 11, 15) + d (2, 5) 6) Design a magnitude comparator to compare two 2-bit mambers A = A, A ₀ and (5) B = B, B. PART B Answer any two full questions, each carries 15 marks. 4 a) Drow the circuit and explain the operation of TTL NAND gate b) Compare TTL, CMOS logic families in terms of fam-in, fam-oxt, supply voltage, propagation delay, power discipation and noise margin 5 a) Implement the following function using PLA F1(x, y, z) = \(\subseteq \text{m} (1, 2, 4, 6) \) F2(x, y, z) = \(\subseteq \text{m} (1, 2, 4, 6) \) F2(x, y, z) = \(\subseteq \text{m} (0, 1, 6, 7) \)		Course Code: £4.207	
Max. Market 100 PART A Answer any two full questions, each corrier 15 marks, (8) (a) Convert the following (b) (AB6), to Decimal (ii) (247.50), into Hexa Decimal (iii) (247.50), into Hexa Decimal (iv) (AF9.B0D)), into Binney (b) Consider the signed binary numbers A = 01000110 and B = 11010011 where B is in 2% completion form, Fact the value of the following mathematical expression (ii) A+B (iii) B-A 2 a) Hamming code was used to generate parity for a nibble. If received bit sequence is 0101010 then write correct bit sequence with (i) Exen parity (ii) Odd parity (ii) Explain the operation of a 8x1 multiplexer and implement the following using an 8x1 multiplexer F(A, B, C, D) = \(\subseteq \text{m} (0, 3, 3, 5, 6, 7, 8, 9, 11, 13, 14) 3 Minimize the following logic function using K- maps and realize using NAND (10) gates alone F(A, B, C, D) = \(\subseteq \text{m} (0, 3, 5, 8, 9, 11, 15) + d (2, 5) (b) Design a magnitude comparator to compare two 2-bit markets A = A, A ₀ and (5) B = B, B. PART B Answer any two full questions, each carries 15 marks. 4 a) Drow the circuit and explain the operation of TTL. NAND gate (b) Compare TTL, CMOS logic families in terms of families, supply voltage, propagation delay, power dissipation and noise margin 5 a) Implement the following function using PLA F1(x, y, z) = \(\subseteq \text{m} (1, 2, 4, 6) \) F2(x, y, z) = \(\subseteq \text{m} (1, 2, 4, 6) \) F2(x, y, z) = \(\subseteq \text{m} (0, 1, 6, 7) \)		Course Name: LOGIC CIRCUIT DESIGN (EC, AE)	-laurs
Answer any two full questions, each corrier 15 marks. (8) (a) (AB6) ₁₀ to Decimal (iii) (545.26) ₁₀ into Octal (iii) (247.38) ₃ into Hexa Decimal (iv) (AF9.B0D) ₁₀ into Binuty Binuty aumbers A = 81000110 and B = (1010011 where B is in 2's completered form, First the value of the following mathematical expression (1) A+B (iii) B-A (a) Hamming code was used to generate parity for a nibble. If received bit sequence is 0101010 then write correct bit sequence with (i) Exen parity (ii) Odd parity h) Explain the operation of a 8x1 multiplexer and implement the following using an 8x1 multiplexer (F(A, B, C, D) = \(\sum \text{(0)} \), 3, 5, 6, 7, 8, 9, 11, 13, 14) (a) Minimize the following logic function using K- maps and realize using NAND (10) gases above F(A, B, C, D) = \(\sum \text{(0)} \) m (0, 3, 5, 8, 9, 11, 15) + d (2, 5) (b) Design a magnitude comparation to compare two 2-bit mathers A = A ₁ A ₀ and (5) B = B ₁ B ₀ PART B Answer any two full questions, each carries 15 marks. (a) Draw the carcuit and explain the operation of TTI. NAND gate (b) Compare TTI, CMOS logic families in terms of families in specify voltage, propagation delay, power dissipation and mose margin (a) Implement the following function using PLA F1(x, y, z) = \(\sum \text{(1, 2, 4, 6)} \) F2(x, y, z) = \(\sum \text{(1, 2, 4, 6)} \) F2(x, y, z) = \(\sum \text{(1, 2, 4, 6)} \) F2(x, y, z) = \(\sum \text{(1, 2, 4, 6)} \) F2(x, y, z) = \(\sum \text{(1, 2, 4, 6)} \)	Man	100000	******
Answer way two full questions, each corries 15 marks. (8) (a) Canvert the following (ii) (AB6) in to Decimal (iii) (347,36); into Hexa Decimal (iv) (AF9,B0D)) into Binney (iii) (AF9,B0D) into (AF9,B		PARTA	400000
(ii) (AB6) ₀ to Decimal (iii) (543.26) ₁₀ into Octal (ii) (247.36) ₁₀ into Hexa Decimal (iv) (AF9.BOD) ₁₀ into Binny		Answer any two full questions, each carries 15 marks.	
(ii) (AB6) ₁₀ to Decimal (iii) (\$43,26) ₁₁ into Octal (iii) (247,36) ₁₅ into Hexa Decimal (iv) (AF9,BOD) ₁₀ into Binary Binary b) Consider the signed binary numbers A = 01000110 and B = 11010011 where B is in 2's completizent form. Find the value of the following mathematical expression (i) A + B (iii) B - A 2 a) Humming code was used to generate parity for a nibble. If received bit sequence is 0101010 then write correct bit sequence with (i) Even parity (ii) Odd parity b) Explain the operation of a 8x1 multiplexer and implement the following using (7) an 8x1 multiplexer F(A, B, C, D) = \(\sum_{10} \) m (0, 3, 3, 5, 6, 7, 8, 9, 11, 13, 14) 3 a) Minimize the following logic function using K-maps and realize using NAND (10) gates alone F(A, B, C, D) = \(\sum_{10} \) m (0, 3, 5, 8, 9, 11, 15) + d (2, 3) b) Design a magnitude comparator to compare two 2-bit mambers A = A ₁ A ₀ and (5) B = B ₁ B ₀ PART B Answer any two full questions, each curries 15 murks. 4 a) Draw the current and explain the operation of TTL NAND gate (10) b) Compare TTL, CMOS logic families in terms of fan-in, fan-out, supply voltage, propagation delay, power discipation and noise margin 5 a) Implement the following function using PLA F1(x, y, x) = \(\sum_{10} \) m (0, 1, 6, 7) Page 1 of 2	29 9	Consent the following	(8):
(ii) (247.36) _k into Hexa Decimal (iv) (AF9.B0D) ₁₆ into Binney b) Consider the signed binney numbers A = 01000110 and B = (1010011 where B is in 2's completeen form. Find the value of the following mathematical expression (i) A+B (ii) B-A (iii) B-A 2 a) Hamming code was used to generate parity for a nibble. If received bit sequence is 0101010 then write correct bit sequence with (i) Exen parity (ii) Odd parity b) Explain the operation of a 8x1 multiplexer and implement the following using an 8x1 multiplexer F(A, B, C, D) = ∑ m (0, 3, 3, 5, 6, 7, 8, 9, 11, 13, 14) 3 a) Minimize the following logic function using K-maps and realize using NAND (10) gates alone F(A, B, C, D) = ∑ m (0, 2, 3, 8, 9, 11, 15) + d (2, 3) b) Design a magnitude comparate to compare two 2-bit mambers A = A ₁ A ₀ and (5) B = B ₁ B ₀ PART B Answer any two full questions, each curries 15 murks. 4 a) Draw the carcuit and explain the operation of TEL NAND gate (10) b) Compare ETL, CMOS logic families in terms of fan-in, fan-ous, supply voltage, propagation delay, power dissipation and mose margin (5) Fig. 7, x) = ∑ m (1, 2, 4, 6) Fig. 7, x) = ∑ m (0, 1, 6, 7) Page 1 of 2		sees year 261 into Cicial	
Binary b) Consider the signed binary numbers A = 01000110 and B = (1010011 where B is in 2°s completeen from, First the value of the following mathematical expression (i) A+B (ii) B-A (iii) B-A 2 a) Hamming code was used to generate parity for a nibble. If received bit sequence is 0101010 then write correct bit sequence with (i) Exen parity (ii) Odd parity b) Explain the operation of a 8x1 multiplexer and implement the following using an 8x1 multiplexer F(A, B, C, D) = \(\sum \text{in} \) (0, 3, 3, 5, 6, 7, 8, 9, 11, 13, 14) 3 a) Minimize the following logic function using K-maps and realize using NAND (10) gates alone F(A, B, C, D) = \(\sum \text{in} \) (0, 2, 3, 8, 9, 11, 15) + d (2, 3) b) Design a magnitude comparation to compare two 2-bit mambers A = A ₁ A ₀ and (5) B = B.B. PART B Answer any two full questions, each curries 15 murks. 4 a) Draw the caroun and explain the operation of TTL NAND gate b) Compare TTL, CMOS logic families in terms of fan-in, fan-out, supply voltage, propagation delay, power dissipation and noise margin 5 a) Implement the following function using PLA F1(x, y, z) = \(\sum \text{in} \) (1, 2, 4, 6) F2(x, y, z) = \(\sum \text{in} \) (1, 2, 4, 6) F2(x, y, z) = \(\sum \text{in} \) (0, 1, 6, 7)			
 b) Consider the signed binary numbers A = 01000110 and B = (1010011 where B is in 2's completion form. Find the value of the following mathematical expression (i) A+B (ii) B-A 2 a) Hamming code was used to generate parity for a nibble. If received bit sequence is 0101010 then write correct bit sequence with (i) Even parity (ii) Odd parity b) Explain the operation of a 8x1 multiplexer and implement the following using an 8x1 multiplexer F(A, B, C, D) = ∑ m (0, 3, 3, 5, 6, 7, 8, 9, 11, 13, 14) 3 a) Minimize the following logic function using K- maps and realize using NAND (10) gates alone F(A, B, C, D) = ∑ m (0, 3, 5, 8, 9, 11, 15) + d (2, 3) b) Design a magnitude comparate to compare two 2-bit numbers A = A₁A₀ and (5) B = B₁B₀ PART B Answer any two full questions, each curries 15 murks. 4 a) Draw the circuit and explain the operation of TTL NAND gate (10) b) Compare TTL CMOS logic families in terms of familie, supply voltage, propagation delay, power discipation and rosse margin a) Implement the following function using PLA F1(x, y, z) = ∑ m (0, 1, 6, 7) Fage 1 of 2 			
 (iii) B - A 2 a) Hamming code was used to generate parity for a nibble. If received bit sequence (8) is 0101010 then write correct bit sequence with (i) Exen parity (ii) Odd parity (b) Explain the operation of a 8x1 multiplexer and implement the following using (7) an 8x1 multiplexer F(A, B, C, D) = ∑ m (0, 3, 3, 5, 6, 7, 8, 9, 11, 13, 14) 2 a) Minimize the following logic function using K- maps and realize using NAND (10) gates alone F(A, B, C, D) = ∑ m (0, 2, 3, 8, 9, 11, 15) + d (2, 5) (b) Design a magnitude comparator to compare two 2-bit mambers A = A₁A₀ and (5) B = B₁B₀ PART B Answer any two full questions, each carries 15 murks. 4 a) Draw the current and explain the operation of TTL NAND gate (10) b) Compare TTL, CMOS logic families in terms of fan-in, fan-out, supply voltage, propagation delay, power discipation and noise margin (10) F1(x, y, x) = ∑ m (1, 2, 4, 6) F2(x, y, z) = ∑ m (0, 1, 6, 7) Fage 1 of 2 		is in 2's complement form. Find the value of the interesting management expression	(7.)
 (8) Hamming code was used to generate parity for a nibble. If received bit sequence is 0101010 then write correct bit sequence with (i) Exen parity (ii) Odd parity (b) Explain the operation of a 8x1 multiplexer and implement the following using an 8x1 multiplexer F(A, B, C, D) = ∑ m (0, 3, 3, 5, 6, 7, 8, 9, 11, 13, 14) (a) Minimize the following logic function using K- maps and realize using NAND (10) gates above F(A, B, C, D) = ∑ m (0, 3, 3, 8, 9, 11, 15) + d (2, 5) (b) Design a magnitude comparator to compare two 2-hit mambers A = A₁A₀ and (5) B = B B. PART B. Answer any two full questions, each carries 15 murks. (a) Draw the current and explain the operation of TTL NAND gate (b) Compare TTL, CMOS logic families in terms of fan-in, fan-cot, supply voltage, propagation delay, power discipation and noise margin (a) Implement the following function using PLA F1(x, y, z) = ∑ m (1, 2, 4, 6) F2(x, y, z) = ∑ m (0, 1, 6, 7) Fage 1 of 2 		(ii) A-B	
is 0101010 then write correct be sequence with (i) Exen parity (ii) Odd parity b) Explain the operation of a 8x1 multiplexer and implement the following using an 8x1 multiplexer F(A, B, C, D) = ∑ m (0, 3, 3, 5, 6, 7, 8, 9, 11, 13, 14) a) Minimize the following logic function using K-maps and realize using NAND (10) gates alone F(A, B, C, D) = ∑ m (0, 3, 5, 8, 9, 11,15) + d (2, 3) b) Design a magnitude comparation to compare two 2-bit mambers A = A, A ₀ and (5) B = B, B ₀ PART B Answer any two full questions, each curries 15 murks. 4 a) Draw the current and explain the operation of TTL NAND gate (10) b) Compare TTL, CMOS logic families in terms of fan-in, fan-ous, supply voltage, propagation delay, power dissipation and moise margin a) Implement the following function using PLA Filex, y, z) = ∑ m (1, 2, 4, 6) Fage 1 of 2			
 h) Explain the operation of a 8x1 multiplexer and implement the following using. (7) an 8x1 multiplexer E(A, B, C, D) = ∑ m(0, 3, 3, 5, 6, 7, 8, 9, 11, 13, 14) a) Minimize the following logic function using K- maps and realize using NAND (10) gates above E(A, B, C, D) = ∑ m(0, 3, 5, 8, 9, 11, 15) + d(2, 3) b) Design a magnitude comparator to compare two 2-bit numbers A = A₁A₀ and (5) B = B₁B₀ PART B Answer any two full questions, each curries 15 murks. 4 a) Draw the current and explain the operation of TTL NAND gate (10) b) Compare TTL, CMOS logic families in terms of fan-in, fan-out, supply voltage, propagation delay, power discipution and mose margin a) Implement the following function using PLA F1(x, y, z) = ∑ m (0, 1, 6, 7) Fage 1 of 2 	2 1		(K)
an 8xt multiplexer F(A, B, C, D) = \(\sum \text{in} \) (0, 3, 3, 5, 6, 7, 8, 9, 11, 13, 14) a) Minimize the following logic function using K- maps and realize using NAND (10) gates alone F(A, B, C, D) = \(\sum \text{in} \) (0, 3, 5, 8, 9, 11, 15) + d (2, 3) b) Design a magnitude comparation to compare two 2-bit mambers \(A = A_1 A_0 \) and (5) \(B = B_1 B_0 \) PART B Answer any two full questions, each curries 15 murks. 4 a) Draw the circuit and explain the operation of TTL NAND gate (10) b) Compare TTL, CMOS logic families in terms of fan-in, fan-out, supply voltage, propagation delay, power dissipation and mose margin a) Implement the following function using PLA (8) \(F1(x, y, z) = \sum \text{in} \text{in} \) (1, 2, 4, 6.7) \(F2(x, y, z) = \sum \text{in} \) (0, 1, 6, 7)			
F(A, B, C, D) = \(\sum \text{in} \((0, 3, 3, 5, 6, 7, 8, 9, 11, 13, 14 \) a) Minimize the following logic function using K- maps and realize using NAND (10) gates alone \[F(A, B, C, D) = \(\sum \text{in} \) in (0, 2, 5, 8, 9, 11, 15) + d (2, 3) b) Design a magnitude comparation to compare two 2-bit mambers \(A = A_1 A_0 \) and (5) \[B = B_1 B_0 \] PART B Answer any two full questions, each curries 15 marks. 4 a) Draw the circuit and explain the operation of TTL NAND gate (10) \[b) \] Compare TTL, CMOS logic families in terms of fan-in, fan-out, supply voltage, propagation delay, power dissipation and mose margin a) Implement the following function using PLA (8) \[F1(x, y, z) = \(\sum \text{in} \) in (1, 2, 4, 6.7) \[Page 1 of 2 \]	1	Explain the operation of a 8x1 multiplexer and implement the following using	(7)
a) Minimize the following logic function using K- maps and realize using NAND (10) gates alone F(A, B, C, D) = ∑ m (0, 3, 3, 8, 9, 11,15) + d (2, 3) b) Design a magnitude comparator to compare two 2-bit mambers A = A ₁ A ₀ and (5) B = B ₁ B ₀ PART B Answer any two full questions, each curries 15 murks. a) Draw the circuit and explain the operation of TTL NAND gate (10) b) Compare TTL CMOS logic families in terms of fan-in, fan-out, supply voltage, propagation delay, power dissipation and noise margin a) Insplement the following function using PLA F1(x, y, z) = ∑ m (1, 2, 4, 6.) F2(x, y, z) = ∑ m (0, 1, 6, 7) Page 1 of 2		an 8x1 multiplexer	
gates alone F(A, B, C, D) = \(\sum (0, 3, 3, 8, 9, 11, 15) + d (2, 3) \) b) Design a magnitude comparator to compare two 2-bit members A = A, A ₀ and (5) B = B, B ₀ PART B Answer any two full questions, each curries 15 murks. a) Draw the circuit and explain the operation of TTL NAND gate (10) b) Compare TTL, CMOS logic families in terms of fan-in, fan-out, supply voltage, propagation delay, power dissipation and noise margin a) Implement the following function using PLA (8) F1(x, y, z) = \(\sum m \) (1, 2, 4, 6.) F2(x, y, z) = \(\sum m \) (0, 1, 6, 7).		$F(A, H, C, D) = \sum m(0, 3, 3, 5, 6, 7, 8, 9, 11, 13, 14)$	
F(A, B, C, D) = ∑ m (0, 3, 5, 8, 9, 11,15) + d (2, 3) b) Design a magnitude comparator to compare two 2-bit mambers A = A ₁ A ₀ and (5) B = B ₁ B ₀ PART B Answer any two full questions, each curries 15 murks. a) Draw the circuit and explain the operation of TTL NAND gate (10) b) Compare TTL, CMOS logic families in terms of fan-in, fan-out, supply voltage, propagation delay, power dissipation and noise margin a) Implement the following function using PLA (8) F1(x, y, z) = ∑ m (1, 2, 4, 6.) F2(x, y, z) = ∑ m (0, 1, 6, 7) Page 1 of 2	3 4	Minimize the following logic function using K- maps and realize using NAND	(10)
 b) Design a magnitude comparator to compare two 2-bit mambers A = A₁A₀ and (5) B = B₁B₀ PART B Answer any two full questions, each carries 15 marks. a) Draw the current and explain the operation of TTL NAND gate (10) b) Compare TTL, CMOS logic families in terms of fan-in, fan-out, supply voltage, propagation delay, power dissopation and noise margin a) Implement the following function using PLA (8) F1(x, y, z) = ∑ m (1, 2, 4, 6.) F2(x, y, z) = ∑ m (0, 1, 6, 7) Page 1 of 2 		gates alone	
B = B ₁ B ₀ Answer any two full questions, each curries 15 murks. 4 a) Draw the circuit and explain the operation of TTL NAND gate (10) b) Compare TTL, CMOS logic families in terms of far-in, fam-out, supply voltage, propagation delay, power dissipation and noise margin 5 a) Implement the following function using PLA (8) F1(x, y, z) = \(\sum_{\text{if}} m \) (1, 2, 4, 6.) F2(x, y, z) = \(\sum_{\text{if}} m \) (0, 1, 6, 7) Page 1 of 2	2	$F_1(A, B, C, D) = \sum m(0, 3, 5, 8, 9, 11, 15) + d(2, 3)$	
PART B Answer any two full questions, each curries 15 marks. 4 a) Draw the circuit and explain the operation of TTL NAND gate (10) b) Compare TTL, CMOS logic families in terms of fan-in, fan-out, supply voltage, propagation delay, power dissipation and noise margin 5 a) Implement the following function using PLA (8) F1(x, y, z) = \(\sum_{\text{if}} m \) (1, 2, 4, 6.) F2(x, y, z) = \(\sum_{\text{if}} m \) (0, 1, 6, 7) Page 1 of 2	6	Design a magnitude comparator to compare two 2-bit numbers A = A ₁ A ₀ and	(5)
Answer any two full questions, each carries 15 marks. 4 a) Draw the circuit and explain the operation of TTL NAND gate (10) b) Compare TTL, CMOS logic families in terms of fan-in, fan-out, supply voltage, propagation delay, power dissipation and noise margins a) Implement the following function using PLA (8) F1(x, y, z) = \(\sum_{\text{if}} m \) (1, 2, 4, 6.) F2(x, y, z) = \(\sum_{\text{if}} m \) (0, 1, 6, 7) Page 1 of 2		$B=B_1B_0$	
 a) Draw the circuit and explain the operation of TTL NAND gate (10) b) Compare TTL, CMOS logic families in terms of fan-in, fan-out, supply voltage, propagation delay, power dissipation and noise margins a) Implement the following function using PLA (8) F1(x, y, z) = ∑ m (1, 2, 4, 6) F2(x, y, z) = ∑ m (0, 1, 6, 7) Page 1 of 2 		7,10017 (10)	
 b) Compare TTL, CMOS logic families in terms of fan-in, fan-out, supply voltage, propagation delay, power dissipation and noise margins a) Implement the following function using PLA (8) F1(x, y, z) = ∑ m (1, 2, 4, 6) F2(x, y, z) = ∑ m (0, 1, 6, 7) Page 1 of 2 			
propagation delay, power dissipation and mose margin 5 a) Implement the following function using PLA $F1(x, y, z) = \sum m(1, 2, 4, 6)$ $F2(x, y, z) = \sum m(0, 1, 6, 7)$ Page 1 of 2			(10)
Fig. 3. Implement the following function using PLA (8) $FI(x,y,z) = \sum_i m(1,2,4,6)$ $F2(x,y,z) = \sum_i m(0,1,6,7)$ Fage 3 of 2			(5)
FI(x, y, z) = \sum m (1, 2, 4, 6) F2(x, y, z) = \sum m (0, 1, 6, 7) Page 1 of 2			
$F2(x, y, z) = \sum_{i=1}^{n} m_{i}(0, 1, 6, 7)$ Page 1 of 2	5 9	Implement the following function using PLA	(8):
Page 1 of 2		$FI(x, y, x) = \sum m(1, 2, 4, 6)$	
		$F2(x, y, z) = \sum_{i=1}^{n} m_{i}(0, 1, 6, 7)$	
		Page 1 of 2	
Scanned by CamSc		Scanned by Co	amSc

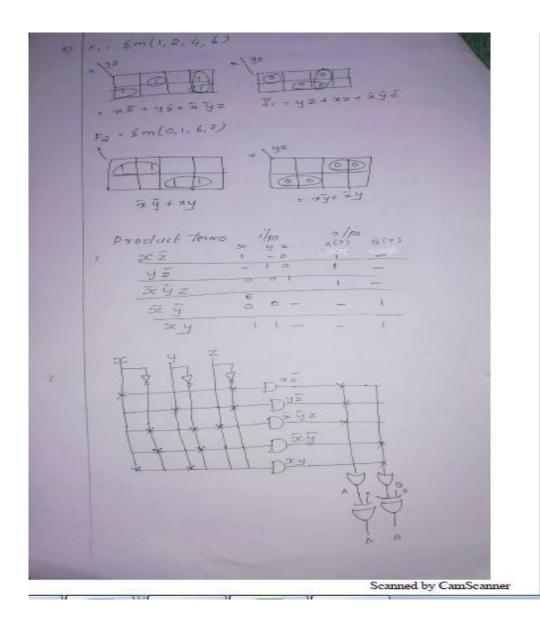


Explains a MOD 6 asynchronous counter using J K Flip Flop Design a 3-bit synchronous counter using D Flip Flop Design a 3-bit synchronous counter using D Flip Flop PART C Auswer any few full questions, each carries 20 marks. The and explain its working b) Explain Moore and Mealy machine models. Compare the models Explain Moore and Mealy machine models. Compare the working with truth table. b) For the given state diagram, design a sequential circuit with D flip flops	(10)
Design a 3-bit synchronous counter using to Pup Prop Domert SR Flip Flop into J K Flip Flop PART C Answer any two full questions, each carries 20 marks. Dow the logic diagram of 3 bit PIPO shift register with LOAD/SHIFT control and explain its working. Explain Moore and Mealy machine models. Compare the models Draw the logic diagram of 3 -bit Johnson counter and explain the working with truth table.	(30) (5) neirol (10) (30) with (10)
b) Convert SR Flip Flop into J K Flip Flop PART C Answer any two full questions, each carries 20 marks. 7 a) Draw the logic diagram of 3 bit PIPO shift register with LOAD/SHIFT conting and explain its working. b) Explain Moore and Mealy machine models. Compare the models 8 a) Draw the logic diagram of 3 -bit Johnson counter and explain the working with truth table.	(5) autrol (10) (10) with (10)
b) Convert SR Flip Flop into J K Flip Flop PART C Answer any two full questions, each carries 20 marks. 7 a) Draw the logic diagram of 3 bit PIPO shift register with LOAD/SHIFT control and explain its working. b) Explain Moore and Mealy machine models. Compare the models 8 a) Draw the logic diagram of 3 -bit Johnson counter and explain the working with truth table.	outrol (10) (10) with (10)
PART C Auswer any two full questions, each carries 20 marks. 7 a) Draw the logic diagram of 3 bit PIPO shift register with LOAD/SHIFT control and explain its working. b) Explain Moore and Mealy machine models. Compare the models. 8 a) Draw the logic diagram of 3—bit Johnson counter and explain the working with truth table.	(10) with (10)
7 a) Draw the logic diagram of 3 bit PIPO shift register with LOAD/SHIFT control and explain its working. 8 a) Draw the logic diagram of 3 -bit Johnson counter and explain the working with troth table.	(10) with (10)
and explain its working b) Explain Moore and Mealy machine models. Compare the models 8 a) Draw the logic diagram of 3 -bit Johnson counter and explain the working with truth table.	(10) with (10)
and explain its working b) Explain Moore and Mealy machine models. Compare the models 8 a) Draw the logic diagram of 5 -bit Johnson counter and explain the working with truth table.	(10) with (10)
Draw the logic diagram of 3 -bit Johnson counter and explain the working with truth table.	
triath table.	
Inith table.	
	(10)
b) For the given state diagram, design a sequential circuit with D flip flops	(10)
 (ii) Obtain the simplified input equations for all input flip flops and i simplified equation for the output. 	nd the
simplified equation for the output. 9 a) Minimize the state table using implication chart.	ed the
simplified equation for the output. 9 a) Minimize the state table using implication chart.	
9 a) Minimize the state table using implication chart. Present Next state Output (Z ₁ Z ₂)	
simplified equation for the output. 9 a) Minimize the state table using implication chart.	
Simplified equation for the output.	
9 a) Minimize the state table using implication chart. Present Next state Output (Z ₁ Z ₂)	
Simplified equation for the output.	
9 a) Minimize the state table using implication chart. Present Next state Output (Z ₁ Z ₂)	
Section Sect	
Simplified equation for the output.	





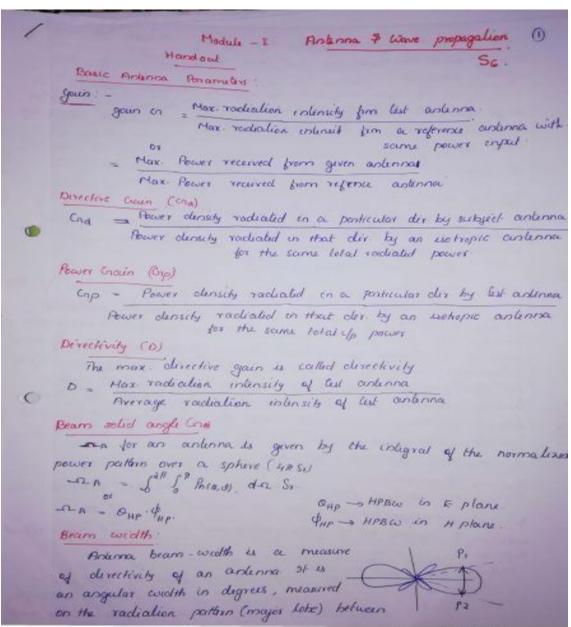




Established in 2001 Managed by Catholic Diocese Kothamangalam

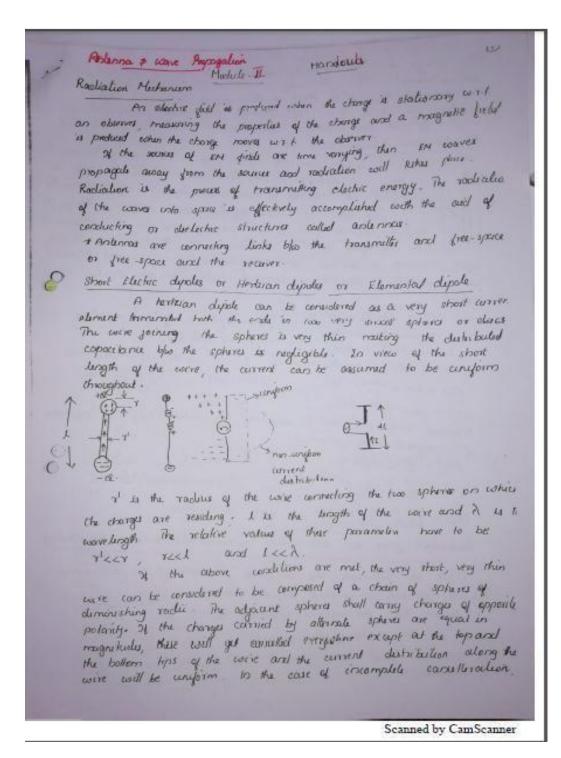


10. Handout Copy



Scanned by CamScanner

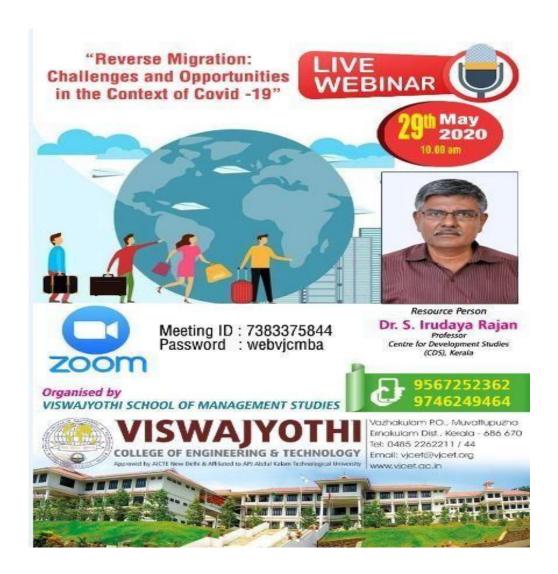




Established in 2001 Managed by Catholic Diocese Kothamangalam



11. Workshops, Talks conducted in VJCET



Established in 2001 Managed by Catholic Diocese Kothamangalam



PROGRAMME SCHEDULE

Welcome Speech: Dr. Shunmugesh K, HOD MED

Resource Person: Mr. Rinto George,

Faculty, Gravitech Inspection Servies,

Ernakulam

Vote of Thanks : Eldose Raju, 58 ME-B

ABOUT THE PROGRAMME

MEP (Mechanical, electrical and plumbing) refers to the aspects of building constructions and design. This is widely used in commercial buildings. In commercial buildings these aspects are often designed by an engineering firm specializing in MEP. MEP design is very important in decision making, accurate documentation, performance and cost estimation, construction planning, managing and operating. Where as HVAC stands for heating, ventilation and air conditioning is the technology of indoor and vehicular environmental control. This machine is primarily designed to take control of the environmental conditions inside the home to provide thermal comfort. HVAC system is designed as a sub discipline of mechanical engineering, based on the principles of thermodynamics, fluid mechanics and heat transfer. HVAC is an important part of residential structures such as buildings, homes, apartments hotels etc. This talk emphasis on importance of mep and hvac in the present world in engineering scenario.

Programme Coordinator: Mr. Abraham Antony,

Assistant Professor, MED

Mr. Nidheesh k.

Assistant Professor, MED

"Moulding Engineers par excellence with integrity, fairness and human values"

AN EXPERT TALK

"Importance of MEP and HVACfor Mechanical Engineers in the Present World"

27th- January - 2020



Venue: class room D420 & D 421 Date: 27-01-2020 (Monday)

Time: 11:00 AM



Organized By,

MECHANICAL ENGINEERING ASSOCIATION

VISWAJYOTHI COLLEGE OF ENGINEERING AND TECHNOLOGY
VAZHAKULAM, MUVATTUPUZHA
ERNAKULAM, KERALA - 686 670



	Date: 27/01/2020		
	Venue: - Some clas	- man (0-	42010 400 38
	Topic :- Expert	F-11 000	102040 1101)
	Resource Elevento	CONTRACTOR IN	E THIVAC
S-No	Name Name	-Kiob nem	ge (Grantech
- STUD		Class	Signature
10	Toyal Abraham	58 ME B	(5)
1	Mehannet Josem Moidern		277
-	Hemoreth Pic		Lightly
4.	Jayarankar		- tarket
5	Fridin Saley	14	(Cho)
- Se	William Eldone		(harden
7-	Atten boy		150 - It -
8	Nother Soby	1 1	Euro L
9	Alon, Markey		de
10	Kishan Paul		Students
11	Fiven targhest	201	Tue
1.7	Titon 2 Olive	***	W.
170	1 1 1	19	20 THE POST
14		1000	Column .
15	Adman Iskin	108	AD .
16	Alphigans Ragu	10.	age -
1-7	Arteny Tehanoan	**	- short
18	Brodgee Bede	0	#8744
19	Alon Binn	12	- CAL
- 65	Mathewa Blenny	11	Mark-
41		10	Weste
- 23	Sugar The Kumen	- 10	april to
23	Birde Samson .	4	4-1-54
84	Agin Man	9	一個完
2.5	Adith Sweet		- Alter-
21	Flain P Charlet		- 100
24	Methin shelly	V	and the same of th
2.8	Scroph Bonney Kudujerickom	77	The state of the s
29	Seahore flagor	4	F-17-00
280	Amal Bayer	At 1	CHAT;
3)	Basil Toy	N. C.	2000 in
32	Mail Strafu	M	
3.7	Jenny Jishiy	1	
			100



move the expenditure for the holowing official place. A copy of the relevant document in correction with a purpose is stacked stong with permission for due leave. TADA to attend workshop/semiparicoal ferences FDP/sementing Registration charges Membership for Development activities Purchaserepter Compressor for the proposal fadditional sheet it necessary) (andly grant permission to conduct Andread Westhop of Selec A&B Students on 9th and 10th March 2020 of a Decemptor Les Necessary ask amplements may be done to insteal Andread and to rether in the system on 7th march 2020. Philosophia and to take in the days of workshop and the students may also be laken on the days of workshop and the students may permitted to use there smart phone inside the R20 Olah was the workshop Sound system also may be averaged. Kindly release the sameticesed amount of De 10000/- lotted in the budget for conducting the workshop. memended by HOD Yours faithfully. From John. AP. ECE	100000000000000000000000000000000000000	cation for Sanction Or	
move the expenditure for the tollowing official pluspose. A copy of the relevant document in connection with purpose is effectively even. TADA to attend workshop/sempedinoe/flerunce/FDP/meeting Registration charges Membership fee Development activities Purchasentaple Compresses Condig grant permission the condent Andreid Wexhapp of Set of 45 Students on get and lok march does of the condent Neurosciple and lok march does of the condent Neurosciple and to the students army as anything the workshop and the students army as anything the south for march 2010 Philosophic and be taken on the days of markshop and the students army as the workshop found the students army permitted to one their smart phone which the R20 Keb will be the workshop found the south of the R20 Keb will be the workshop found the south of the south of the students army and the workshop found the south of the south	May I request you to kindly gra	nt permocion/accord sanction for a	sum of Rs
TADA to attend workshop/sempetricofferences FDP/sementing Registration charges Membershop toe Development actives Perchassingste Compresses Siffication for the proposal fadditional sheet it necessary) Cody grant permission to conduct Android Workshop of Set of 46 Students on 9th and 10th March 2010 of in Set of 46 Students on 9th and 10th March 2010 of in Neurolay are anythered may be dead to inskall Android and to the system of 7th march 2010 Philosophic and be taken on the days of workshop and the students any permitted to one their smart phone middle the R20 (leab permitted to one their smart phone middle the R20 (leab with workshop Semid Egilentials in ay to averaged. Kindly release the nonchioned company of the workshop. Membershop The budget for conducting the workshop. The budget for conducting the workshop. Wours faithfully. Director Sent & Signature	Rupees		
Responsible to Development actives Purchaseneppie Commission for the proposal fadditional sheet it necessary) Cody grant permission to conduct Android we skelp on a set of A & Students on get and 10k march 2010 of 10 conful to Neurosay as amperiods may be done to inskall Android which in the system on 7th march 2010. Philosophic and be laken so the days of workshop and the student may be be laken so the days of workshop and the student may be permitted to use their smart phone inside the R20 (ket) permitted to use their smart phone inside the R20 (ket) permitted to use the sometimes of the accordance of the student for permitted to use the sometimes of the accordance of the student for conducting the workshop. I kindly reliance the sametimes demount of Discool-letted in the budget for conducting the workshop. I kindly the budget for conducting the workshop. The principal principal Director Seal & Signature	2 meet the expenditure for the follows he purpose is attached along with per	ng official plurpose. A copy of the reli mission for duty leave.	evant document in connection with
Membership to Development actives Purchaseneper Compression for the proposal (additional sheet if necessary) Condy grant permission to conduct Android Workshop Os SEEC 18 6. Students on 9th and 10th March 2020 of Is Disorbit to the system on 7th march 2020 Philosophic and be taken on the days of workshop and the students may be taken on the days of workshop and the students may permitted to one there smart phone incide the R20 (leab and the acceptance small system also may be concerned.) Northly release the nanctioned amount of Ps. 100001- letted in the budget for conducting the workshop. In the budget for conducting the workshop. The budget for conducting the workshop and the budget for conducting the workshop.	=	ricofference#CPImeeting	
Development acquires Purchaseneper Comparation communiar events Other principal Confidence of the proposal fadditional sheet it necessary) Kindly grant permission he condend Android Workshop On 36 fc A& B Students on 9th and 10th march 2010 of Is D confident his Necessary are anythered may be dead to make all Android and to the fire anythered may be dead to make all Android and to the fire anythered on the students may age be taken on the days of morehashop and the students may age the workshop small syllim, also may be arranged. Kindly release the sameticesed amount of the 1000cl- letted in the budget for coodering the workshop. The fire the budget for seedenting the workshop. The fire the f			
Compression contests avents Compression for the proposal fadditional sheet if necessary) Condy grant permission to conduct Android Workshop Or Seek A& & Students on att and 10K March 2020 of 10 complete to Necessary are amperisals may be don't to instable Android Necessary are amperisals may be don't to instable Android and to the system on the march 2020. Philosophia and be taken on the days of workshop and the students may permitted to one their smart phone inside the REO (lab arrive the workshop found systemation may be averaged. Visingly reliance the samplement armount of the 1000cf- lotted in the budget for conducting the workshop. The workshop for the days of System Emperiore. Principal Sould Signature Sould Signature Sould Signature Sould Signature Sould Signature			
Congression for the proposal (additional sheet if necessary) Kindly grant permission to conduct Android Workshop Or SEEC AS 6. Students on 9th and 10th March 2020 of Is Discovered to the system on 9th march 2020 of India mather in the system on 7th march 2020. Philosophia and be baken on the days of consisting and the students may permitted to one their smoot phone imide the R20 Olah as the workshop Sound systematics may be accompact. I Kindly release the sameticaned amount of R2 10000f- letted in the budget for conducting the workshop.	Purchasairage		
Condy grant permission to conduct Android Workshop or Sete As & students on 9th and 10th March 2020 of Necessary are anyonests may be dient to suskable Android Necessary are anyonests may be dient to suskable Android ndio methor in the eyelism on 7th march 2020. Photographic and to taken on the days of workshop and the students only Opermitted to one their smart phone inside the 220 leab as a the workshop Sound system also may be assumpted. Nendly release the samplement armount of 12s 10000/- lotted in the budget for conducting the workshop. Interest to the budget for conducting the workshop. The budget for conducting the workshop the workshop. The budget for conducting the workshop th	Cumoular co-cumoular events		1
Condy grant permission to conduct Andread Workshop of Setic AS B. Students on 9th and 10th March 2020 of It is computed to the system on 7th march 2020. Philographs and to take in the system on 7th march 2020. Philographs and be taken on the days of workshop and the students may as be taken on the days of workshop and the students may as the workshop found system also may be assumpted. Vising the workshop found system also may be assumpted. Vising the budget for condenting the workshop. Intel in the budget for condenting the workshop. Wours faithfully. Finally Frincipal Capture Director System Emperature Soul & Signature	Otruprevents		
Condy grant permission to conduct Andread Workshop of Setic AS B. Students on 9th and 10th March 2020 of It is computed to the system on 7th march 2020. Philographs and to take in the system on 7th march 2020. Philographs and be taken on the days of workshop and the students may as be taken on the days of workshop and the students may as the workshop found system also may be assumpted. Vising the workshop found system also may be assumpted. Vising the budget for condenting the workshop. Intel in the budget for condenting the workshop. Wours faithfully. Finally Frincipal Capture Director System Emperature Soul & Signature	stification for the proposal (addit	local sheet if naces and	
of Sete As 6. Students on 9th and 10th March 2020 of 10 0 confinence are angenerals may be don't to instable Andrew Mechanics in the eyelens on 7th march 2020. Philosophic and be taken on the days of societation and the students may on permitted to one there snout phone inside the R20 leable and the workshop Sound system, also may be amonged. I kindly release the sametioned amount of R2 10000/-letted in the budget for conducting the workshop. Wours faithfully. From the Cythia Control of System Engineers The PRO 9 System Engineers Sould Signature Director Seal & Signature Sould Signature Sould Signature Sould Signature Sould Signature Sould Signature Sould Signature	Kindly grant permiss	sion to conduit An	decid Workshop
and to the system on 7th march 2010. Philosophia as be Eaken on the days of workshop and the students may be presented to one their smart phone incide the 220 Keep wing the workshop small system. The march of 12 10000/- Intid in the budget for conducting the workshop. Intid in the budget for conducting the workshop. In the Captal Topy To PRO & System Englished. AP. ECE Name & Signature Director Sould Signature Director Sould Signature Sould Signature Sould Signature Sould Signature	tox seec AFB, stud	lents on 9th and 1	ok march 2020 de
and to the system on 7th march 2010. Philosophia as be Eaken on the days of workshop and the students may be presented to one their smart phone incide the 220 Keep wing the workshop small system. The march of 12 10000/- Intid in the budget for conducting the workshop. Intid in the budget for conducting the workshop. In the Captal Topy To PRO & System Englished. AP. ECE Name & Signature Director Sould Signature Director Sould Signature Sould Signature Sould Signature Sould Signature	NED COMPANIES as and	ements may be dent	To unkall Adam
og be kaken on the days of workshop and the students ormy permitted to one there smart phone inside the R20 Clab as so the workshop Sound system also may be averaged. I knowly release the sometimed amount of 12: 10000/- lotted in the budget for conducting the workshop. I works Gultist Tooks Gultist Copy to PRO & Syster Emperson Principal South Signature Director South Signature South Signature South Signature South Signature	the dia the	system of 7th ma	ich sua Ohmanh
Special that he was office small phone mide the 120 0000 will be southed by the workshop. Whindly release the sometimed amount of 12 100001-letted in the budget for conducting the workshop. Manual Special Capture of System Englished Ap. ECE Name & Signature of staff Director Seed & Signature	tudio mens	Person marketing	dotte students man
mmended by HOD Yours faithfully. From K.E. Griffeld: Topy To PRO & Systim Emperous Principal Seed & Signature Director Seed & Signature	ogy be taken on the	day of motestip a	mide the RED ORAL
mmended by HOD Yours faithfully. From K.E. Griffeld: Topy To PRO & Systim Emperous Principal Seed & Signature Director Seed & Signature	e permitted to one	Franch States She was he	ansampech.
mmended by HOD Yours faithfully. From K.E. Griffeld: Topy To PRO & Systim Emperous Principal Seed & Signature Director Seed & Signature	Kindle whose of	he sametimed and	sunt of the world
Tracks Capted tioned by: Opy To PRO & System Empress Principal Director Seed & Signature	Hotted in the budget	for readult as other	continue
Tonks Cyfrid PRO & Systine Empresser A Director Seed & Signature Director Seed & Signature Seed & Signature Seed & Signature Seed & Signature	area	The second of the	- race mayer
Seal & Signature Seal & Signature Soal & Signature	ommended by HOD		Yours faithfully,
Seal & Signature Seal & Signature Soal & Signature	an-		AND DESCRIPTION OF THE PARTY OF
Seal & Signature Seal & Signature Soal & Signature	The Control		Euro John, AP. ECE
Seal & Signature Seal & Signature Soal & Signature	ctioned by :	N	ame & Signature of staff
Seal & Signature Seal & Signature Soal & Signature	(20)	y to PKO4 System Em	fe weez
Seal & Signature Seal & Signature Soal & Signature		700300	
See & Signature See & Signature See & Signature	A18-	LVML	
Forwarded to AO/FO for necessary action.	ALB-	Director	Manager
Forwarded to AQ/FO for necessary action.	Commonpair.	Director	manager
Porwarded to ACIFO for necessary action.	17 A III I I I I I I I I I I I I I I I I	Director	manager
	Seaf & Signature	Seal & Signature	Seal & Signature
	Seaf & Signature	Seal & Signature	Seal & Signature
	Seaf & Signature	Seal & Signature	Seal & Signature
	Seef & Signature	Seal & Signature	Seal & Signature



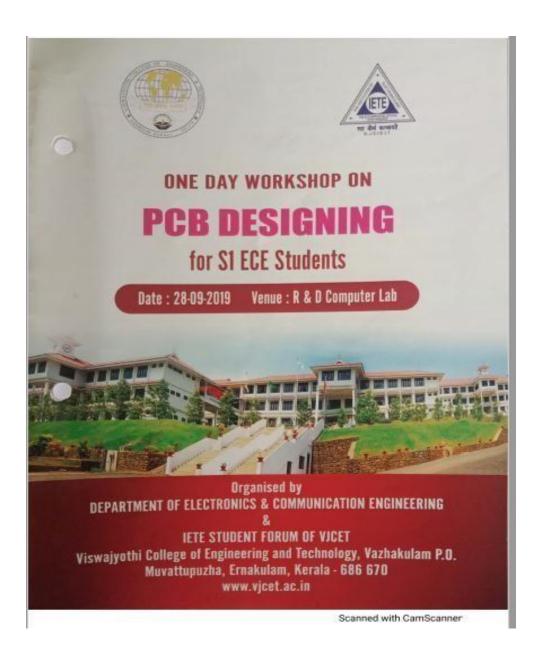


Android workshop on 9.3.2020



1 3 4 5	AATHRA A MENON AISWARYA S NAIR AKHL SAJU ALAN JOSE	The	Marke	兴	July -
3 4 5	AISWARYA S NAIR AXHIL SAJU ALAN JOSE	The	MA	2	Nu cont
4 5 n	AKHIL SAJU ALAN JOSE	Achil	Medical	AND DE	A STATE OF THE STA
5-	ALAN JOSE	CALIFORNIA .		1110	2000
10.				L. M.	Provi
	ALPHONSA RENNY	2	36	Sc.	R.
7	ANGELA SUNNY	120	101	1661	AND
8	ANJITH P.N	disc -	1	100	4
9	ANU SHALET PHILIP	Antabl	Ashall	ANGOLL	- British
10	ARYACS	di-	-bogs	24	-24
11	ARYADEVIK V	A.	de.	do.	do
13	BASIL KOCHUPURACKAL	Pull S	Roll	Version	1000
5	DEVAVRATHAN'S	THE STATE OF THE S	Carre	100	Columb
8	GOURINANDANA N	Clark	Eget.	God	CHER.
9	GREESHMA GEORGE	Harris .	Marks.	I sest of	Monto
0	HARISANKAR S	1 out this	11151090	1 No	Ilanda -
1	JESS MATHEW	-64	F Sel		15.00
2	LAKSHMIPRIYA B	Land	Zakk	Zuice:	we
3	MARIA CELAS THOMAS	ALC:	Miles	Copples	P. Service
	MARIA THERESA	James	1	Jan	100
5	MARIYA POLSON	POWER	CK	Marin.	654
	MINALEE SIBI	Maria	Madde	40	VILE
_	NEENU SHOBY	AS-	X8_	100	TNI-
_		W.	452	60.	8a
_	The state of the s	Rose	226	Webs-	POGL
_		0.0	E.Ja	Quite	8 kc
-		1		10	1
-		100	100	101.00	- Trans
	100 111 113 115 115 18 9 0 0 12 2 5 4	ARYACS ARYADEVIK V BASIL KOCHUPURACKAL BASIL KOCHUPURACKAL BEVAVRATHAN S GOURINANDANA N GREESIBMA GEORGE HARISANKAR S JESS MATHEW LAKSHMIPRIYA B MARIA CELAS THOMAS MARIA THERESA MARIYA POLSON MINALEE SIBI NEENU SHOBY RADHIKA C A RAHUL SATHYAN SRUTHY VARGHESE SUSAN RANJU	ID ARYACS II ARYADEVIK V II BASIL KOCHUPURACKAL II BASIL KOCHUPURACKAL II BEVAVRATHAN S II GOURINANDANA N II GESHMA GEORGE II HARISANKAR S II JESS MATHEW II LAKSHMIPRIYA H II MARIA CELAS THOMAS II MARIA THERESA II MARIYA POLSON II MINALEE SIBII II NEENU SHOBY II RADHIKA C A II RAHUL SATHYAN II SRUTHY VARGHESE SUSAN RANJU	ID ARYACS II ARYADEVIK V II BASIL KOCHUPURACKAL IS DEVAVRATHAN S B GOURINANDANA N 9 GREESHMA GEORGE 10 HARISANKAR S I JESS MATHEW 2 LAKSHMIPRIYA B 3 MARIA CELAS THOMAS B MARIA THERESA 5 MARIYA POLSON MINALEE SIBI NEENU SHOBY RADHIKA C A RAHUL SATHYAN SRUTHY VARGHESE SUSAN RANJU	ID ARYACS II ARYADEVIK V III BASIL KOCHUPURACKAL III BASIL KOCHUPURA





Established in 2001

Scanned with CamScanner



VISWAJYOTHI COLLEGE OF ENGINEERING & TECHNOLOGY DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING VOUCHER Rs.1400 - has been spent for the one day workshop on PCB desinging organized by IETE Students Forum conducted on 28/9/2019 as honorarium to the resource person Mr. Krishnendu K. VJCET, Vazhakulam





40			ate: 28/09/2019 Signature
SI. No.	Name	class	Phid
And in concession to	ABHIN MANOS	S1-666	
	DEHISIM M.A	SI-EEE	Alkan
	July Jus	SJ-KCE	1000
	Nakul-B	SEEE	9
	Never But But	5,-161	Newsper
	Kieling & Bija	S, ECE	Budge
	Egila M. Eldho	S, 606	Right
	Birty Abraham	S, ECE - A	Budes
	Alla Paulose	SIECE A	146
	Samardhi Sunil Inamdan	SIECEA	Sandhi.
	Sullma 3	SIECEN	4
	BOOK STATE OF THE	S. ECE A	Contiana
	Nordhana P. Royesh	SI ECE B	80
	Provide Pradeep	Sieres	Box
	Rohan Bisoy	S. ECE'S	Pohy
			8
	Akahan Sankers ! P	S, ECE-B	
	Tony John		The second secon
18	HRISHI VENKITESHIM	SIECE-A	
	Bruth: Salkyan	SIECEA	Outh
20			

Established in 2001 Managed by Catholic Diocese Kothamangalam



12. Placement cell Activities

Placement cell of the college organizes training which includes quantitative aptitude and soft skills. Technical value added courses are given to the students based on their interests and learning ability.

		Cell Activities	
	Year 20	019-2020	-
SINo	Name of Add on /Certificate programs offered	Number of students enrolled in the year	Number of Students completing the course in the year
1	Aptitude	510	406
2	Technical Training Python Domain	158	145
3	Resut	40	32
4	Soft Skills Training	227	172
4	Soft Skills Learning Soft Skills Learning MUVATUPUZHA KERALA	Vir. C. Mavier AP & PO	172



Established in 2001 Managed by Catholic Diocese Kothamangalam



Konfidence

33/740-C, Link Retreat, Vennala P.O., Kochi 682028.

Phone: 94472 35913, 94479 78265, 99470 66609

www.konfidenceonline.com

Email: KonfidenceOnline@gmail.com

Viswajyothi College of Engineering: Aptitude Training by Konfidence; 2016 - 20 Batch Attendance

SI No	Name	Branch	16-Mar-19	01-May-19	11-May-19	01-Jul-19	02-Jul-19	03-Jul-19	23-Aug-19	24-Aug-19	17-Sep-19	27-Sep-19
1	Abhinand S	CE	A	×	x	A	х	×	x	×	x	×
2	Abraham Regi	CE	A	Α	A	A	A	A	A	A	A	A
3	Abrin Samson .	CE	A	x	х	x	×	A	×	×	×	х
4	Adarsh Mathew	CE	А	A	A	A	×	×	×	x	×	×
5	Adharsh Unnikrishnan	CE	А	х	А	x	x	A	x	A	×	×
6	Adwaith B	CE	А	x	x	A	x	x	×	×	×	×
7	Afshan Nizar	CE	А	А	А	А	А	А	A	Α	A	A
8	Ajeena Baby	CE	А	х	х	x	x	А	×	х	х	x
9	Ajin John	CE	А	×	x	А	×	х	x	х	×	x
10	Aju J George	CE	Α	х	х	х	х	А	х	x	×	х
11	Ajwin Jose Francis	CE	А	x	А	А	х	Α	x	А	х	x
12	Akash Jose	CE	Α	Α	А	А	А	А	А	А	А	А
13	Akash Venu	CE	А	x	х	х	х	х	х	А	х	х
14	Akhil Sunil	CE	А	А	А	А	А	А	A	Α	А	А
15	Alan Mathew	CE	А	х	х	х	х	х .	х	Α	х	х
16	Albin Antony	CE	х	Α	х	х	х	х	х	А	х	х
17	Albin Sunny	CE	Α	х	x	Α	А	А	х	х	х	х
18	Almitha James Pooveli	CE	Α	Α	Α	Α	Α	Α	А	А	А	А
19	Amala Thomas	CE	Α	х	х	х	х	*	×	А	х	х
20	Amil Mohan*	CE	х	Α	х	х	x//	KO?	N'XO	х	А	х
21	Amitha Emmanuel	CE	х	х	х	х	100	X20	XZ	x	х	х
22	Anandhu Soman	CE	х	х	А	х	X/2	A	OXM	x	х	х
23	Ancy John	CE	Α	Α	x	х	A	350	8	х	А	А
24	Aneena Wilson	CE	Α	Α	х	х	x	А	х	A	х	х
25	Angel Roy	CE	Α	Α	Α	Α	А	A	А	A	A	A
26	Anish Sudarsan	CE	Α	Α	Α	Α	А	Α	Α	A	A	A
27	Anitta Thomas	CE	х	х	х	х	х	х	х	x	X	х
28	Anjana Jayakumar	CE	Α	Α	Α	А	A	A	A	A	A	A

Profe-

MUVATTUPUZHA

Established in 2001





OVERALL DATA Attendence summary of Technical Training (Python)								
ATTENDED	AT LEAST 2 DAYS	AT LEAST 3 DAYS	AT LEAST 5 DAYS	AT LEAST 8 SESSIONS				
ADVANCED LAB	60	52	51	51				
BASIC LAB	11	- 11	11	11				
INTERMEDIATE A	38	38	38	38				
INTERMEDIATE B	49	49	45	45				
OVERALL STUDENTS	158	150	145	145				



AP & PO



Established in 2001





U R SOLUTIONS

No. 22/5, Benson Road, Benson Town,
Bangalore - 560 046.
M: 9845199314
e-mail: info@ursolns.com
www.ursolns.com

Soft Skill Training by U R SOLUTIONS 2016-2020 Batch Batch - A (PTC Hall)

SI.No		Class & Branch	29th July 2019	30th July 2019	31st July 2019	1St August 2019
1	ABY MATHEWS	CSE	A	Α	A	A
2	Aishwarya G Prabhu	CSE	P	P	P	P
3	Akhil George	CSE	P	P	P	P
4	Akshaya Thomas	CSE	P	P	P	P
5	Aleena Aloysius	CSE	P	P.	P	P
6	Aleena Paulose	CSE	P	P	P	P
7	ALEENA SANTO	ECE	P	P	A	P
8	AMAL JOSEPH	ECE	P	A	A	A
9	Ananthu Santhosh	CSE	P	P	P	P
10	ANITEJ	ECE	P	P	P	P
11	Anjana S	ECE	P	P	P	A
12	Anju Joly	ECE	Р	P	A	P
13	Anju Susan Kuriakose	CSE	P	Р	P	P
14	Anna Maria George	CSE	Р	P	P	P
15	Ano Jai	CSE	Р	P	P	P
16	Anu Maria Sunny	ECE	Р	P	A	A
17	ARYA KS	ECB	Р	P	P	A
18	Ashish S Pillai	CSE	A	A	A	A
19	BENJAMIN'BABY JACOB	ECE	Р	P	Р	P
20	Ceril Joseph	ECE	Р	P.	A	A
21	CHITHIRA MAHESH	ECE	Р	Р	Р	Р
22	CHRISTO JOJO	ECE	Р	Р	Р	Р
23	DANY JOJI	ECB	Р	Р	Р	Α
24	Deepak Benny	CSE	A	A	A	A
25	Dolby Vincent	CSE	Р	A	A	Α
26	Febin Emmanuel	CSE	Α	A	A	A
27	Geethu Sony	ECE	Р	Р	A	А
28	George Mathew	CSE	Р	Р	Р	P
29	Georgekutty Jose	CSE	Р	Р	Р	Р
30	Gloya Xavier	ECE	Р	Р	A	A
31	Greeshma Raj	ECE	Р	Р	A	A
32	Harsha P H	CSE	Р	Р	Р	Р
33	JAYASANKAR K	ME	Р	Р	Р	Р
34	Jeena Paul	CSE	Р	Р	P	Р
35	JEEVAN GEORDY	ME	Р	Р	Р	Р
36	JEFFIN JOSE	ECE	Р	Р	Р	Р

MUVATTUPUZHA KERALA

Established in 2001 Managed by Catholic Diocese Kothamangalam



13. Club Activities



VISWAJYOTHI COLLEGE F ENGINEERING AND TECHNOLOGY, VAZHAKULAM

INDUSTRY INSTITUTE INTERACTION CELL

SUBMISSION

19th November 2020

Permission may be granted to conduct a Webinar on "How to frame a startup policy". The webinar will be handled by Mr Gautham, Founder and Director-Pupilfirst. This webinar is scheduled to be on 21st November, Saturday from 4.00 PM to 5.00 PM through Google Meet. This webinar is intended to the members of NISP,R&D,IEDC and IIIC cell of VJCET. This is organized by National Innovation and Start Up Policy committee(NISP), Research and Development Division (R&D), Innovation and Entrepreneurship Development Centre (IEDC) and Industry Institute Interaction Cell (CSE,IT dept.) of VJCET.

Mr Vinoj K(Convener-NISP, CORDINATOR-IIIC, IEDC)

Dr K K Rajan

AnishinRaj M M (Dean,R&D)

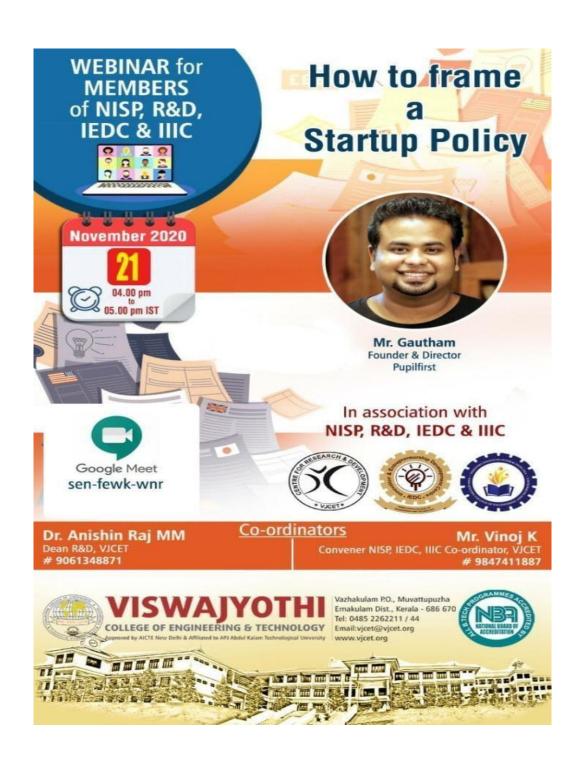
Principal

Mrs. Diana Baby(IT Dept Incharge,IIIC)

Mrs. Remya Paul(CSE Dept Incharge,IIIC)

Fer

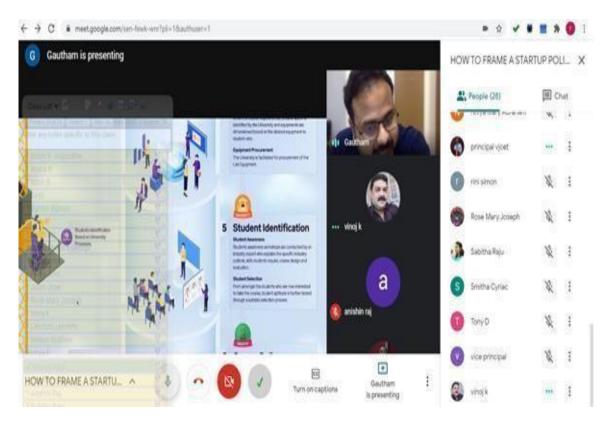




Established in 2001 Managed by Catholic Diocese Kothamangalam



The main objective of this webinar is to get guidelines for framing a startup policy and to know how to improve entrepreneurial skills and abilities among students



Screen shot of the event

Established in 2001 Managed by Catholic Diocese Kothamangalam

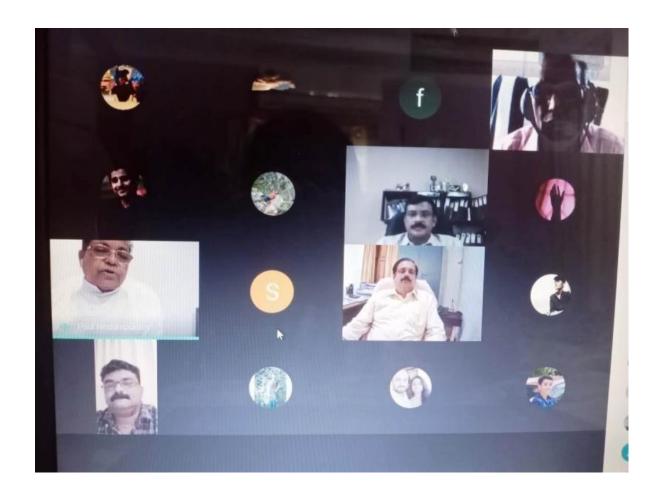




Established in 2001



On 21st August 2020, a live webinar was organised by IEDC in association with R&D, VJCET. This auspicious event commenced at 3 pm.



Established in 2001



14. Lab Manual Copy

VISWAJYOTHI COLLEGE OF ENGINEERING & TECHNOLOGY

VAZHAKULAM, MUVATTUPUZHA - 686670 TEL - 048502262211, 2262255, 2262977



DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

ELECTRONICS DEVICES AND CIRCUITS LAB STUDENTSS LAB MANUAL (EC 231)

Semester: 3

APJ Abdul Kalam Technological University

Established in 2001



Electronics devices and Circuits Lab

CONTENTS

	REGULAR EXPERIMENTS					
Sl. No.	Name of Experiment	Cycle	Page No.			
1.	Diode Characteristics		3			
2.	Bridge Rectifier		10			
3.	3. RC Low Pass and High Pass Circuits as Integrator and Differentiator					
4.	4. Clipping Circuits					
5.	5. Clamping Circuits					
6.	Zener Voltage Regulator		37			
7.	Common Emitter Characteristics		42			
8.	8. Common Emitter RC Coupled Amplifier					
9.	9. RC Phase Shift Oscillator using Transistor					
10.	Transistor Series Voltage Regulator	п	62			
11.	Schmitt Trigger		68			
12.	Colpitt's Oscillators		74			
13.	Astable Multivibrator					
14.	Monostable Multivibrator		82			

Established in 2001



Electronics devices and Circuits Lab

	ADVANCED EXPERIMENTS						
1.	Transistor Series Voltage Regulator 86						
2.	Multivibrators using 555 Timer 91						
	DESIGN EXPERIMENTS						
1.	RC Coupled Amplifier with Gain 50 96						
	OPEN ENDED EXPERIMENTS						
1.	Circuit to turn ON and turn OFF the LEDs for 1 sec each	101					
2.	DC Power Supply	103					

- Sample Viva Questions I.
- II. Sample University Questions

Established in 2001 Managed by Catholic Diocese Kothamangalam



Electronics Devices and Circuits Lab

ADVANCED EXPERIMENTS

Transistor Series Voltage Regulator

<u>Aim</u>: -

a)To design and set up a series voltage regulator to regulate an input voltage of $15 \pm 5 \mathrm{V}$ to an output of 10 V, 500 mA.

b) To plot its line and load regulation.

Components / equipments required: -

SI. No	Components / equipments	Specification	Quantity

Theory: -

A voltage regulator is designed to maintain the output voltage of a power supply constant against the variations of input voltage, changes of load or changes in temperature. Figure shows a two transistor series voltage regulator. In this circuit, transistor TI is a series pass element which functions as an emitter follower and T2 functions as a voltage comparator and a dc amplifier.

SVR functions as a closed loop control system. Suppose the load voltage rises due to the variations in the input voltage, then the voltage at the base of T 2 increases. Since the emitter potential of T2 is held constant by a zener diode, its base to emitter voltage increases. Then its collector current increases collector potential decreases. Since TI acts an emitter follower, emitter potential of T1 follows the potential at its base. Fall in emitter potential of transistor T1offset the initial increase in load voltage.

Established in 2001 Managed by Catholic Diocese Kothamangalam



Electronics Devices and Circuits Lab

Conversely, if the load voltage decreases, base potential of T2 decreases and its emitter potential increases. So any attempt in the change of load voltage is compensated by negative feedback. Since more voltage gets dropped across the transistor, power transistor is used as the series pass element. A heat sink need to be attached with the transistor if the load current is high.

Procedure: -

- 1. Design the circuit.
- 2. Connect the circuit on bread board.
- 3. To plot line regulation characteristics
 - a) Keep the load current at constant value, say 10mA.
 - b) Vary the input voltage from 7 $\rm V$ to 12 $\rm V$ and note down the corresponding output voltage.
 - c) Plot line regulation characteristics with V_{in} along X-axis and V_{out} along Y-axis.
- 4. To plot load regulation characteristics
 - a) Keep the input voltage constant, say 10 V.
 - b) Vary the load current from 10 to 20mA by varying R_L and note down the corresponding output voltage.
 - Plot the load regulation characteristics with I_Lalong X-axis and V_{out} along Yaxis.

Design:

Output requirements $V_0 = 10 \text{ V}$, $I_L = 500 \text{ mA}$ when $Vin = 15 \pm 5 \text{ V}$

Selection of transistors: Select the transistors 2N3055 as T_1 since it is a power transistor and BC 107 as T_2 since it is an error amplifier.

Selection of zener diode: The reference voltage is taken such that $V_z = V_0/2 = 10 \text{ V}/2 = 5 \text{ V}$.

Select 5.6 V zener.

Design of R2:

Assume I₁<<I_L since it is a sampling current, Take I₁=10 mA

Assume $I_D = 10 \text{ mA}$ for the zener to get sufficient current.

87

Established in 2001



Electronics Devices and Circuits Lab

 $V_{R2} = I_1 * R_2$ (I_B is negligible).

 $I_1*R_2 = V_z + V_{be2}$

 $R_2 =$

Designof R1:

 $\mathrm{V}_{o} {=} \, \mathrm{V}_{R1} + \mathrm{V}_{R2}$

So, $V_{RI} = V_o - V_{R2}$

 $I_1R_1 = V_{RI}$. Then $R_I =$.

Design of RD:

 $V_Z + V_{RD} = V_0$

So, $V_{RD} = V_o - V_z$

 $I_DR_D = V_{RD}$. So, RD=

Design of R3:

 $\mathbf{I}_{E1} = \mathbf{I}_L + \mathbf{I}_1 + \mathbf{I}_D$

 I_{B1} = Base current of T_{I} = I_{E1} / $(1 + h_{FE})$ = 25 mA. Since minimum h_{FE} = 20

 $I_3 = I_{B1} + I_{C2},$

Assume $I_{C2} = 2 \text{ mA}$.

Then $I_3 =$

Now $V_i = V_{R3} + V_{BE} + V_o$

So, $V_{R3} = V_i - V_{BE} - V_o$

 $1_3 R_3 = V_{R3}$

So, R3=

Design of RL:

 $R_L = V_o / l_L =$

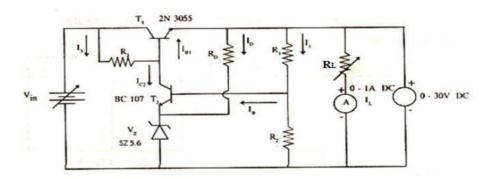
88

Established in 2001 Managed by Catholic Diocese Kothamangalam

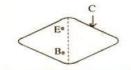


Electronics Devices and Circuits Lab

Circuitdiagram: -

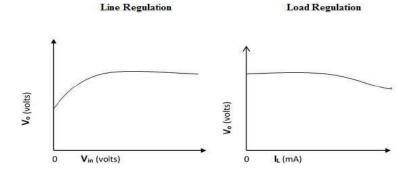


Pin Diagram of 2N 3055: -



Pin out diagram 2N 3055

Expected characteristics: -



Established in 2001



Electronics Devices and Circuits Lab

Observations:-

Line Regulation

I _L =10mA		
Vin (V)	Vo(V)	

Load Regulation

Vin=10V		
$I_L(mA)$	Vo(V)	

Result: -

Established in 2001 Managed by Catholic Diocese Kothamangalam



Electronics Devices and Circuits Lab

DESIGN EXPERIMENTS

Common Emitter RC Coupled Amplifier

Aim:-

To design and set up a common emitter RC coupled amplifier with a mid-band voltage gain of 50.

Components / equipments required:-

Sl. No	Components / equipments	Specification	Quantity

Theory:-

In common emitter amplifier, AC input signal to be amplified is applied between base and emitter terminals. The output is taken from the collector through the coupling capacitor. The emitter-base junction must be forward biased and the collector-base junction must be reverse biased for the proper functioning of a transistor as an amplifier.Base current controls the collector current of a common emitter amplifier. A small variation of base current makes a large variation in the collector current by a factor β . It gives a faithful amplification of input AC signal. For a distortion-less output the operating point must be fixed at the middle of the load line by selecting $V_{CE} = 50\%$ of V_{CC} .

Resistors R_1 and R_2 provide necessary biasing for the circuit. They form voltage divider biasing which requires only one power supply. The voltage across R_2 i.e. $V_{R_2} = V_{CC} \frac{R_2}{R_1 + R_2}$ is used to forward bias emitter base junction. V_{CC} through R_C reverse biases

Established in 2001 Managed by Catholic Diocese Kothamangalam



Electronics Devices and Circuits Lab

OPEN ENDED EXPERIMENTS

Q1. Design a circuit to turn ON and turn OFF the LEDs for 1 sec each.

Solution:-

This can be obtained by designing an astable multivibrator for an ON and OFF duration of 1 sec.

Theory:-

Astable multivibrator is capable of producing square wave for given frequency, amplitude and duty cycle. The output of the circuit forced to swing repetitively between positive saturation +Vsat and negative saturation -Vsat resulting in a square wave output. This circuit is also called free running multivibrator or square wave generator. One transistor will remain in ON state for 1 sec and LEDs in that branch will glow, while other transistor and LEDs are in OFF state. This cycle continues.

Procedure:-

- 1. Design the circuit as per the required specification.
- 2. Connect the circuit on the bread board.
- 3. Switch ON the power supply and observe the output.

Design:-

Let
$$V_{CC} = 12V$$
, $I_C = 10mA$, $\beta = 100$
Forward resistance of LED = 150 Ω

Design of Rc1 and Rc2:

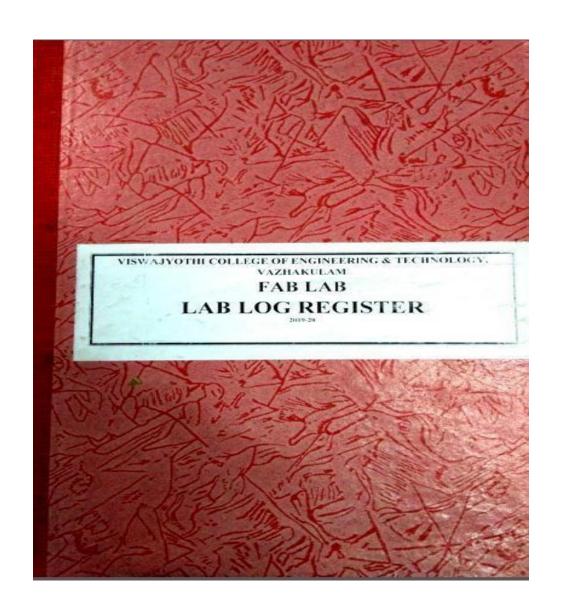
$$\begin{split} & \mathrm{Vcc} - (3 \text{ x } 150 \text{ Ic}) - \mathrm{V_{RC1}} - \mathrm{V_{CE(sat)}} = 0 \\ & \mathrm{V_{RC1}} = \mathrm{Vcc} - (3 \text{ x} 150 \text{ x } 10 \text{ x } 10^{-3}) - \mathrm{VcE(sat)} \\ & \mathrm{R_{C1}} = \mathrm{V_{RC1}} \ / \ \mathrm{Ic} \\ & \mathrm{Take} \ \mathrm{R_{C1}} = \mathrm{R_{C2}} \\ & \mathrm{I_B} = 5 \mathrm{I_C} \ / \ \beta \end{split}$$

101

Established in 2001



15. Activities in FAB LAB



Established in 2001



47	Mapping 111	Trecora Brice	#
-M-	XX -	*Anyare	7
	Class en S	vano Parishage for SI EC-B.	on 3-10-2019.
BAL NO.	St ECO.		dhe
-	SECR	Asira Gebege Louis	dies
3	€ 60 8	Abulay Bankon P	AL P
-	0.00	ALBIN SABU	Alle
8	\$ 56.8	Abaitla Marin	Smille
4	87918	Ann Maria Vined	that the same of t
100.00	494 2	Ann May James	aller.
	250	Mby Jose	Alex
The same of	-	Albieni —	
*	2800	Axyo Marches	10%-
	100	Ashik Gunge	Ada
Section 1	Stea	Ashly Joshey	adiy

				nr 3
	-		(Date: 08-10-19
\$1 No1	class	Rell Not	Name	Signature
13	15, 600	13		Maria
14	SECB	- 14	Bagil Benny	P
15	Sit cis	15	Berson John	Per
16	SECB	16	Bijila M Eldho	- Birde
17	\$1,600B	17	Browence P.A	Beat.
18	SI ECE I		Biyanke Mani	light
19	51, ECEB	19	Botsit Baju	Briggs 8
20	S1,ECEB		Devika Subash	Detale
21	S. FEB	21	Dinu Joy	Spines .
22	SIECEB	12	Edwin Siby	Glieb.
23	S. ECEB	23	Fine James	- Fran
24	SIECE	24	Imvan khan	Down
-25	SIECEB	25	Jibin Joy	Tipo.
26	S. ECB	26	Joe P.B	and .
27	S, ECB	47	Joyal Johnson	اسا

Established in 2001



3
13 05.19. CYBATHLON - 2020 LL: 30 H13. TEAM BUILDING PEMEETING
L-30 Has CYBATHLON - 2020
TEAM BUILDING P MEETING
Participants.
Mr. Ralph Schneider P.J.M.
1.112. ITUNA CIENCE ECE
TUNITAL D.R. MED AND
. Cities & mathew men
mr. Jekson Cronge ECED de
m. Krishnerda K. ECE Kh.
Rahal Sathyan Ecc. 35, The
Physical Division of the Company of
Rost Montin Tom FCE as Ce Garil Joseph GCE AS CE Anontha Krishnam ECEASC A
Annu Man Karal of The Asi Charles
Adareh Tong. Ecco Sr day
Josephi Borgodi Duch
Jessy mathew Ser. Haw Sankas. S ECE-B Su Mathew.
Havi Sankas. S ECE-B Su Mandales.
meeting showled at 2 us to with a Presonlation
of Cybathon solo Information. Design is
explained by Mo. Rollin and the requirements
are also presented to the portet opants. Studies
explained by Mo. Rolph and the requirements are also presented to the porterior of Stedent and to beenly discussed about the possibility of Design dandopment. It is decided to
meet everyday at tablab and proceed
with his ideas at trab lab. Anestry
constanted at 4.pm.

Established in 2001 Managed by Catholic Diocese Kothamangalam





Established in 2001





Cybathlon Team